WHITE PAPER

By integrating commercially developed processing and high speed digitization at chip scale, new microelectronic devices are poised to accelerate the latest defense applications

TOM SMELKER
VP and GM, Microelectronics,
Mercury Systems

TONY TRINH
Senior Director of Project
Management, Microelectronics,
Mercury Systems

The New SiP Device Drives a Leap in RF Edge Processing

The 21st century electronic battlefield is a rapidly evolving arena; this is especially true for systems operating within the RF spectrum. We face adversaries who are using stealthy techniques and deploying advanced weapons systems. Countering those techniques and weapons requires extremely low-latency responses driven by intelligent, adaptive applications. At a practical level, that means there must be a quantum leap in RF processing inserted at the tactical edge.

An injection of new technology is needed, but it is not sufficient. Long-term success demands a continual process that moves innovations from the broad world of commercial electronics into the defense domain. Sustained success also requires that the technology innovations delivered to defense programs come from trusted and secure sources; security threats posed by semiconductor tampering are equal to those posed by software breaches and are more difficult to detect.

There is a dynamic new answer to the RF edge processing challenge, an adaptation of system-in-package (SiP) technology: the RFSiP. The RFSiP combines powerful, multi-function processing with industry-leading analog-to-digital and digital-to-analog (ADC/DAC) capability.

Our technology partnerships, with Xilinx and others, helped us create a high-end mixed signal solution that is packaged in a form factor one fifth the size of a small printed circuit board.

This paper focuses largely on the RFSiP, discussing details of why it's needed, how it functions and where it fits. However, the larger issues of accessible technology and trusted sourcing will also be presented, as they are vital considerations when developing the RFSiP approach.

NEXT-GEN RADAR AND EW NEED HIGH-PERFORMANCE RF EDGE PROCESSING

Electronic warfare is moving to a new level of complexity. High-frequency radars now use pulse widths that last only nanoseconds. In addition to single frequency bursts, frequency-hopping signals are showing up across the RF spectrum. Other techniques include dynamically changing waveforms and patterns.

To reliably detect these stealthy signals, our EW systems must use higher and higher sampling rates so ever-expanding bandwidths can be continuously monitored. Five GS/sec was recently considered a very high sampling rate; now the bar is set at 50 GS/sec.

Detection is just the first step. Effective responses must then be made with extremely low latency, which requires powerful real-time processing for signal analysis and countermeasure generation, all tightly coupled with the ADC/DAC function. A new generation of applications needs very high rates of data conversion and powerful processing that can keep up with those data rates.

A clear example is radar spoofing, where embedded components detect, alter and then replay radar pulses to create false and deceptively moving targets. This only works when the response latency is so low the original emitter radar system cannot perceive a time lag in the replayed pulse. Effectiveness is also dependent on a high spectral density spread across multiple channels to maximize rapid pulse detection and response, making high-fidelity data just as critical as low- latency.

Exploiting Leading-Edge Commercial Technology

The enormous worldwide commercial electronics market continually drives technology forward at a rapid pace with hundreds of billions in R&D investments every year.

The much smaller defense electronics marketplace capitalizes on that significant commercial investment by adopting new technologies, then adapting them to the unique requirements posed by defense applications.

The challenge for defense electronics is to compress the adopt-and-adapt cycle as much as possible. If our defense forces can rapidly access new technologies, we can maintain an advantage over adversaries. We lose that advantage if it takes half a decade to move new technology into deployment.

Mercury is the leader in adapting commercial technology to defense applications and platforms, making them more affordable, safe and secure. We are accelerating the process of bringing new technology to our defense customers as we bridge the gap between commercial technology and defense solutions.

Through close collaboration with our technology teams at Xilinx, Jariet and Ferric, we have been able to adopt the SiP concept and rapidly adapt it for RF edge processing. Likewise, collaboration with the semiconductor industry enables us to integrate latest-generation technologies and push server-class processing to the tactical edge.

Active radars have similar requirements. For example, a multifunction AESA radar puts tremendous demands on embedded processing, as it must dynamically shift from surveillance of long-range threats to tracking and jamming short-range targets. The inherent flexibility of this type of system can only be exploited when all the available data is processed within stringent real-time parameters.

New, still-evolving application areas are adding further processing requirements. Cognitive radar applies artificial intelligence (AI) techniques to extract information about a target from a received signal and then uses that information to improve transmit parameters such as frequency, waveform shape and pulse repetition frequency. In a similar fashion, cognitive EW applies AI to identify patterns in detected data and then develop an appropriate response.

To be effective, both cognitive radar and cognitive EW must execute their AI algorithms in near real-time. That, in turn, requires that graphics processing units (GPUs) are added to the RF processing function, complementing the FPGAs that perform signal analysis and creation. Until recently, multiple processing methods required multiple, distinct semiconductors, often in a multi-board system. New technology has driven past that barrier. (See the description below of the Xilinx Versal® AI Edge ACAP.)

For RF applications, moving data from the ADC/DAC function to a centralized computing resource impacts both data fidelity and latency. The current generation of ADCs/DACs are already generating data bandwidths that overwhelm system-level interconnects, forcing substantial data reduction before processing. The interconnects also introduce transmission times that make the next generation of sophisticated, low-latency radar and EW responses difficult, or impossible

To overcome these limitations, modern designs must move away from a centralized computing model and put all the processing where the data is—at the tactical edge.

OBSTACLES: COMPONENT INTEGRATION AND SWAP

Implementing RF edge processing requires multiple, tightly integrated functions that work together to capture, analyze and manipulate a data stream in real time. Latency requirements favor ADCs/DACs that can implement direct digital conversion. Efficient processing of the digital bit stream demands pipelined operations by some combination of FPGAs, GPUs and general-purpose processors.

All these components must be connected with high-bandwidth interconnects that meet latency needs and be supplied with their required power specifications, all within a package small enough to be placed near the sensing antenna.

A FLEXIBLE APPROACH TO DESIGNING SMALL MULTI-FUNCTION ELECTRONICS

The internet-of-things (IoT) is driving commercial electronics with ever-increasing demands for miniaturization and higher functionality at less cost and lower power. Many-core processors are not the answer; while they can execute billions of instructions per second, they are not designed for optimal power use. They also need support from mixed signal chips and FPGAs for any RF interfaces, making a complete solution into a board-level product.

To meet the IoT's most demanding requirements, microelectronics designers are moving to heterogeneous integration (HI) of SiP technology. This innovative semiconductor design approach connects small units, called chiplets, on a tiny piece of silicon. Each chiplet is designed to perform a specific function, such as RF capture and transmission, ADC/DAC conversion, digital I/O, FPGA-based digital signal processing or any one of the dozens of tasks needed to implement a mixed signal data flow. Every chiplet is an individual semiconductor; they can even be complex, multicore processors.

Chiplets can be selected, combined and connected in many different ways, each combination optimized for a specific application. The results are extremely high-performance solutions that put the multi-function, pipelined dataflow concepts of a printed circuit board onto a very small form factor.

Let's examine a SiP created specifically for RF sensor data processing, and its semiconductor chiplets, each selected to function as part of a cutting-edge solution.

HI SIP DESIGN FOR RF EDGE PROCESSING

Mercury has adapted the HI SiP design approach to meet the rigorous requirements of RF edge processing, and is developing a family of RFSiPs that take technology from the commercial world and make it defense-ready. The description on the next page is focused on a specific RFSiP, the RFS1140.

Trusted Sourcing is Essential

Now, more than ever, leading edge microelectronics are critical to giving our forces a significant technical advantage.

MADE IN USA

One part of maintaining that advantage is ensuring trust and security in the microelectronics supply chain.

The risks in a compromised supply chain are clear. Semiconductor tampering is extremely difficult to detect. It includes things like remotely operated 'kill switches' and hidden 'backdoors.' While many cybersecurity discussions focus on software threats, semiconductor vulnerabilities may present even greater risks. This is a serious, ongoing danger to DoD programs.

Mercury is committed to uncompromised delivery of trusted solutions. We continue to invest in scalable manufacturing operations in the U.S. to enable rapid, cost-effective deployment of our microelectronics and secure processing solutions to our customers. This strategy allows us to assist our customers in reducing program cost, minimizing technical risk, staying on schedule and on budget, and ensuring trust and security in the supply chain.

With regard to the RFSiP specifically, it will be delivered to DoD programs using trusted onshore design, complemented by DMEA-certified manufacturing and testing facilities.

Mercury's Phoenix, AZ production facility

THE VERSAL® AI EDGE ACAP

The RFSiP's processing chiplet represents a new type of semiconductor architecture, an Adaptive Compute Acceleration Platform (ACAP). The Versal® AI Edge ACAP from Xilinx isn't just another FPGA or MPSoC. It's a true heterogeneous processor, fabricated with cutting-edge 7 nm technology and incorporating three different types of compute engines.

Each ACAP device includes Scalar Processors, Programmable Logic and Vector Processors, all connected by an extremely high-bandwidth network-on-chip (NoC). Multiple compute engine types are designed into the ACAP because no single style of processing is capable of optimally performing all the tasks involved in a sophisticated edge application.

Scalar Processors, functioning like traditional CPUs, are ideal for complex decision-making and control. In the AI Edge ACAP, there are four of these: two low-power ARM® Cortex®-R5F real-time processors and two full-power domain Cortex-A72 cores, supported by a system memory management unit.

Programmable Logic, also referred to as Adaptable Engines, adds the flexibility to handle a diverse set of computationally demanding algorithms. Included are FPGA structures, with 1.5 times the LUTs of a high-end Virtex chip, as well as programmable I/O and a customizable memory hierarchy of block RAM and UltraRAM.

Vector Processors, called Intelligent Engines in the AI Edge ACAP, are optimized for advanced signal processing, such as linear algebra and matrix math, which are well suited for 5G wireless systems and AI inference. The chip contains two types: (1) DSP Engines, which function like traditional digital signal processors, and (2) AI engines, similar to advanced GPUs, comprising vector processors for fixed and floating-point operations, a scalar processor and dedicated program and data memories.

In total, a single Versal ACAP chip provides 400 AI engines, 1968 DSP engines and over 900K FPGA LUTs.

THE JARIET ELECTRA-MA ADC/DAC

On the RFSiP, high-end processing power is combined with the extremely fast ADC/DAC capability delivered by the Jariet Electra-MA from Jariet Technologies. Each RFSiP has two of these ultra-low-power transceivers, combining to provide 4 ADC receive channels and 4 DAC transmit channels, all operating at up to 64 GS/s. They can directly digitize frequencies through 36 GHz and operate in the first Nyquist zone up to 32 GHz.

THE FERRIC POWER CONVERTER

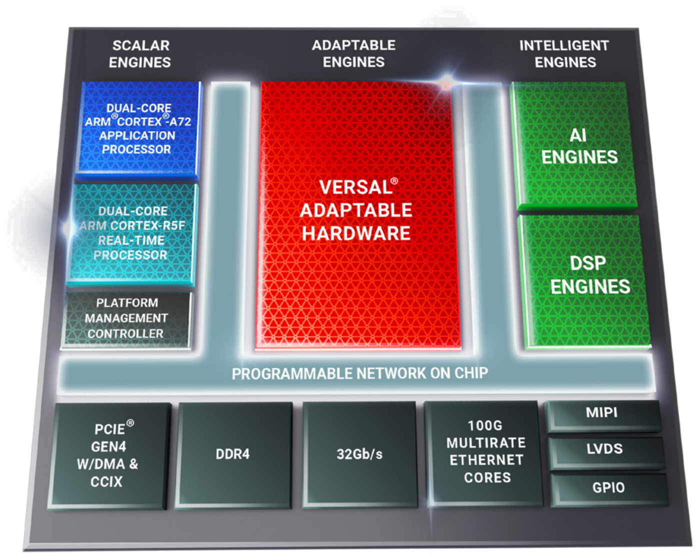
The Ferric power converter is a tiny die power regulator that supports a high current density. Three of these unique chips are configured within the RFSiP, allowing it to take in just a single voltage and break it down for all the voltage rails needed by the other components. This simplified power characteristic makes for straightforward integration into larger systems.

INTEGRATED INTO A TINY FORM FACTOR

The Xilinx, Jariet and Ferric chips, plus 4 GB of DDR4 memory, are all integrated on an organic substrate with a tiny, 50 x 50 mm form factor. The individual chips are integrated using thermal compression bonding, which heats and compresses the dies to make connections. High-bandwidth component interconnections include a dedicated bus, which moves data directly between the Jariet ADC/DACs and the Versal ACAP.

ENABLING HUGE LEAPS FOR RF EDGE APPLICATIONS

The RFSiP provides direct digitization at extremely high sampling rates so systems can detect and monitor the various forms of stealthy signals. By eliminating any need for downconverting to an intermediate frequency (IF), direct digitization helps the RFSiP achieve extremely low latency responses even at 64 GS/s data rates. The RFSiP also meets the massive processing requirements for low-latency responses and for tracking all manner of potential targets, including those moving at hypersonic speeds.



Versal AI Core. Source: Xilinx

This advanced RF application capability is delivered in a SWaP-C optimized package. Functionality equivalent to multiple boards in today's deployed systems is reduced to a single, small package, enabling effective operation in constrained spaces at the tactical edge and lowering overall system costs.

Within the RFSiP, the Xilinx Versal ACAP houses an extensive set of heterogeneous math processing engines, supporting multiple type of computing. They deliver both the raw power and the flexibility needed by AI-based cognitive radar and cognitive EW applications.

Using the SiP design structure also means future generations of semiconductors, created by continuous commercial electronics R&D investments, can be used for rapid upgrades, meaning RFSiP-based applications will be able to add new capabilities in the same physical form factor. (See the sidebar on page three on Exploiting Leading Edge Commercial Technology.)

ENGAGE WITH US

At Mercury, we know that all of our technology innovations are complemented and enhanced by strategic customer relationships, collaborating to solve problems. We see close cooperation with technology visionaries, program managers and engineering teams as key to getting the maximum value from our new RFSiP solutions.

Engage with our team to explore how they can meet your most demanding requirements for RF edge processing and help move your programs forward.

About Mercury

Mercury Systems (Nasdaq: MRCY) is a leading technology company serving the aerospace and defense industry, positioned at the intersection of high tech and defense. Headquartered in Andover, MA, we deliver solutions that power a broad range of aerospace and defense programs, optimized for mission success in some of the most challenging and demanding environments. We envision, create and deliver innovative technology solutions purpose-built to meet our customers' most-pressing high-tech needs.

Corporate Headquarters

50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International

Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 51 00 tel

Learn more:

mrcy.com/chip-scale