New!

Flexor

GateXpress

GateFlow

ReadyFlow
Board Support Package

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: _VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)_
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 5973 is a high-performance 3U OpenVPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

When used with Pentek's gigabit serial copper or optical interface FMCs, the 5973 becomes a high speed data streaming and processing interface. Its built-in data capture and playback features and Gen. 3 x8 PCIe interface make it a turnkey solution.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions That Include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications

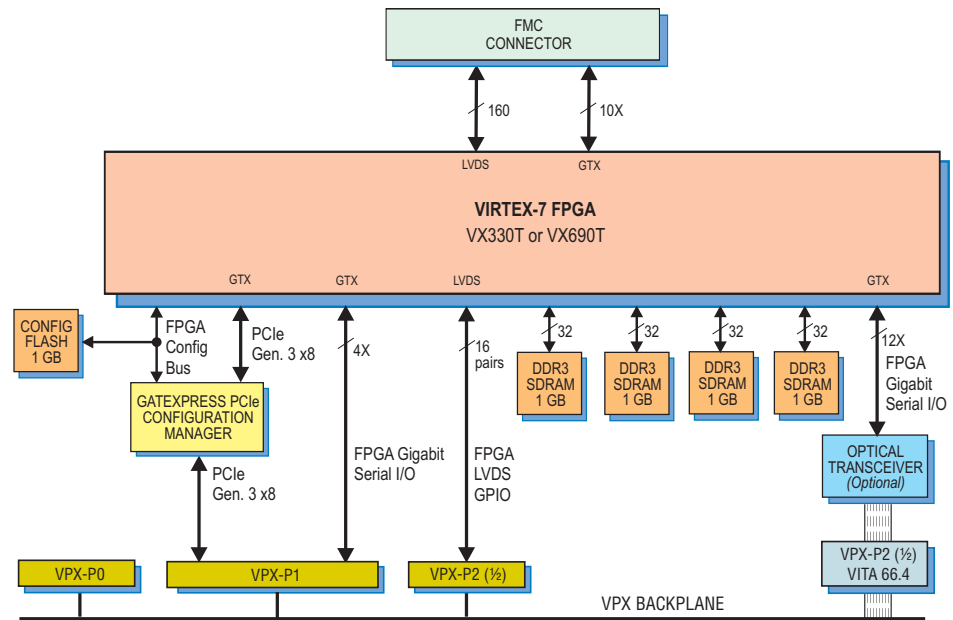where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own. ➤

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK
Development Systems

Ordering Information

Model	Description
5973	3U OpenVPX Virtex-7 Processor and FMC Carrier

Options:

-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

Xilinx Virtex-7 FPGA

The 5973 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5973 supports the emerging VITA-66.4 standard, that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The 5973 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Specifications

I/O Module Interface: VITA-57.1 FMC site
Field Programmable Gate Array
    Standard: Xilinx Virtex-7 XC7VX330T-2
    Optional: Xilinx Virtex-7 XC7VX690T-2
Custom FPGA I/O
    Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
    Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
    Optical: VITA-66.4, 12X duplex lanes
Memory
    Type: DDR3 SDRAM
    Size: Four banks, 1 GB each
    Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
    PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)