



Model 53621 COTS (left) and rugged version



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Optional LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53621 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53621 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

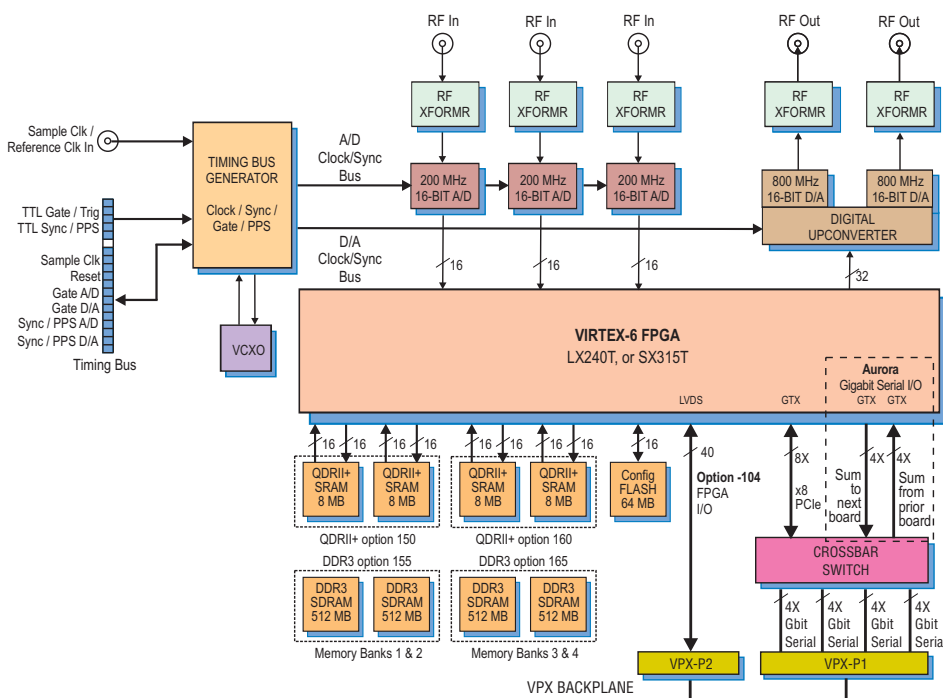
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ▶



A/D Acquisition IP Modules

The 53621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency

setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Beamformer IP Core

In addition to the DDCs, the 53621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average

power level of any DDC core falls below or exceeds a programmable threshold.

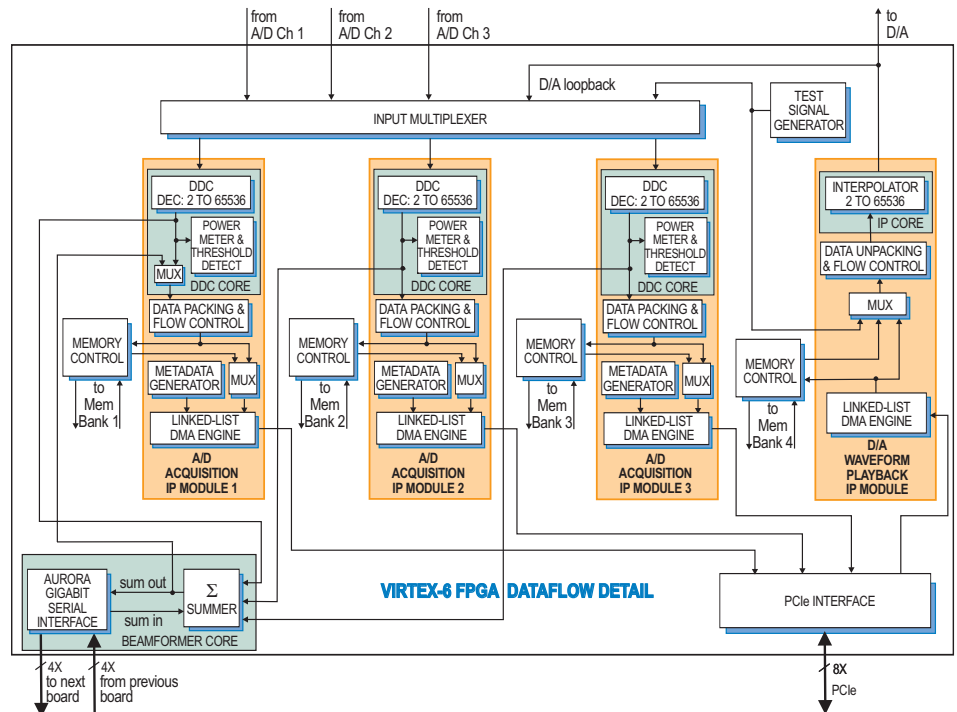
A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53621's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory .

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming. ➤



► A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TIDAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53621 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits ►

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.



Ordering Information

Model	Description
53621	3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U XMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VXSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

► **Digital Downconverters**

Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator

Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer

Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs

Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VXSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8;
 Gen. 2: x4

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

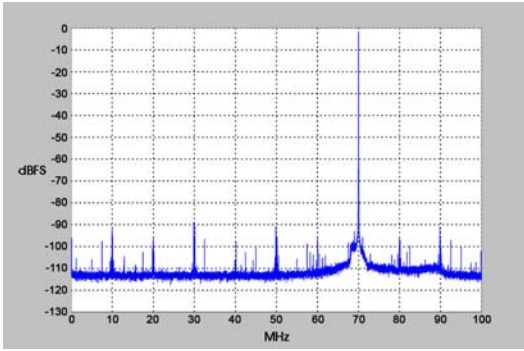
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

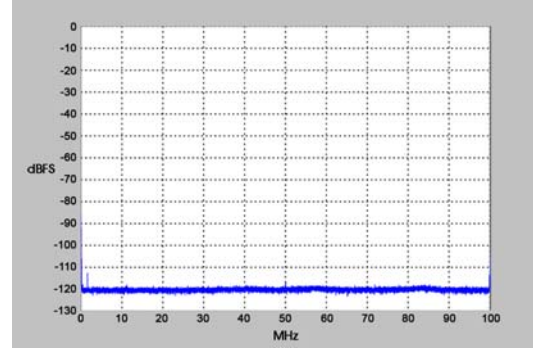
A/D Performance

Spurious Free Dynamic Range



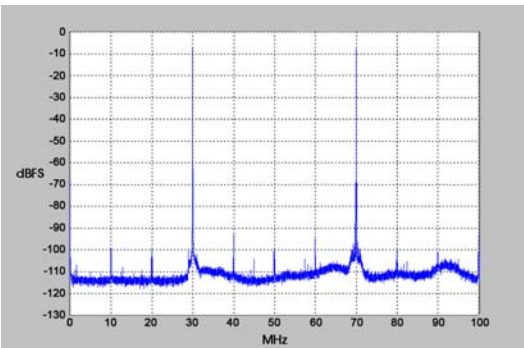
$f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

Spurious Pick-up



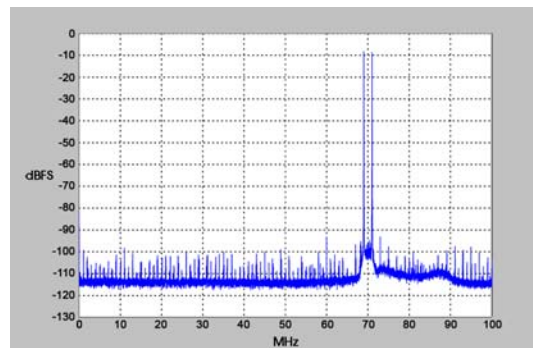
$f_s = 200 \text{ MHz}, \text{Internal Clock}$

Two-Tone SFDR



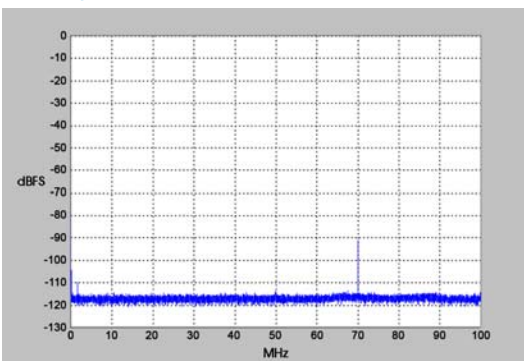
$f_1 = 30 \text{ MHz}, f_2 = 70 \text{ MHz}, f_s = 200 \text{ MHz}$

Two-Tone SFDR



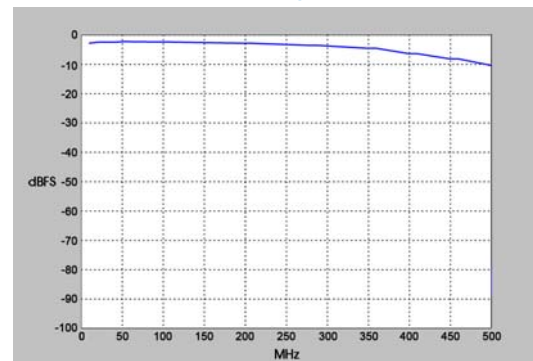
$f_1 = 69 \text{ MHz}, f_2 = 71 \text{ MHz}, f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



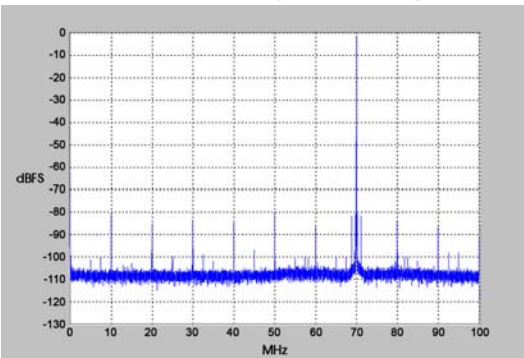
$f_{in \text{ Ch2}} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Ch 1 shown}$

Input Frequency Response



$f_s = 200 \text{ MHz}, \text{Internal Clock}$

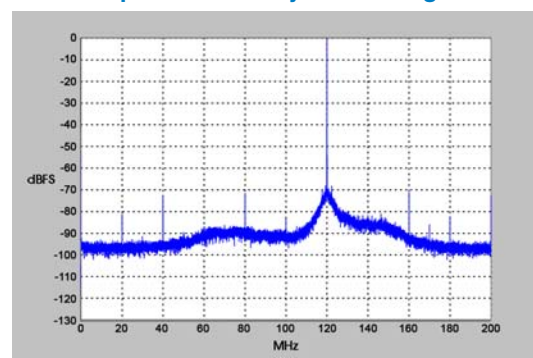
Spurious Free Dynamic Range



$f_{out} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

D/A Performance

Spurious Free Dynamic Range



$f_{out} = 140 \text{ MHz}, f_s = 400 \text{ MHz}, \text{External Clock}$