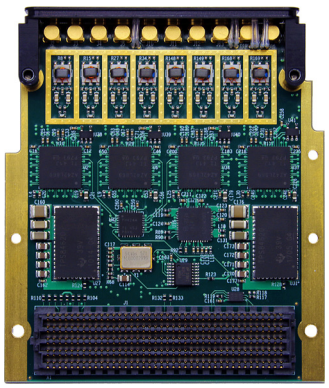
New!

Model 3324

4-Ch. 500 MHz, 16-bit A/D, 4-Ch. 2 GHz, 16-bit D/A-FMC



FlexOr

ReadyFlow Board Support Package

GateFlow

Features

- Four 500 MHz, 16-bit A/Ds
- Four digital upconverters
- Four 2 MHz, 16-bit D/As (500 MHz input data rate, 2 GHz output sample rate with interpolation)
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 3324 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe FMC Carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

Unlocking the True Performance of the Model 3324

The Model 3324 is shipped with a simple Xilinx Vivado project for operating the FMC with the Xilinx VC707 Evaluation Kit. This project includes IP for initializing the FMC and confirming data paths, providing the user with a tested platform for creating their own FPGA IP for operating the FMC.

While users will find the Model 3324 an excellent analog interface to the VC707 or any compatible FMC carrier, the true performance of the 3324 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers.With factory installed IP, the board set provides a turnkey data acquisition and signal generation subsystem, eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition engines, D/A waveform playback engines, programmable linked-list DMA engines, and a metadata-packet creator.

A/D Acquisition IP Modules

When the 3324 is used with a Pentek FMC carrier, the board-set features four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

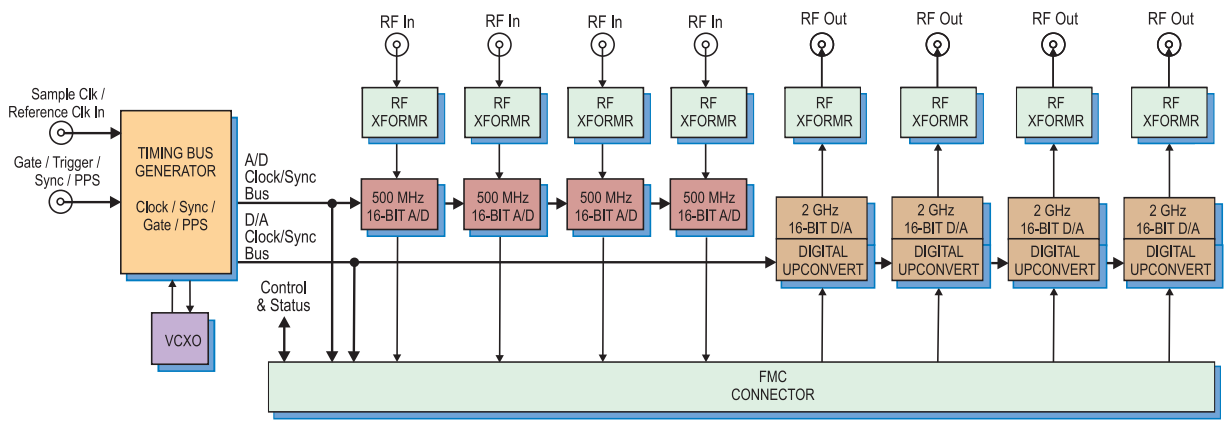
These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform IP Modules

When used with a Pentek FMC carrier, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming. ➤



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Model 3324 — 4-Ch. 500 MHz, 16-bit A/D, 4-Ch. 2 GHz, 16-bit D/A-FMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

FMC Product Combinations

If you wish to purchase this FMC module in combination with an FMC carrier, please see:

- FlexorSet Model 5973-324
- FlexorSet Model 7070-324

Ordering Information

Model	Description
3324	4-Channel 500 MHz, 16-bit A/D, 4-Channel 2 GHz, 16-bit D/A - FMC

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options
8267	VPX Development System See 8267 Datasheet for Options

➤ D/A Converters

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized and create larger multiboard systems.

ReadyFlow Board Support Package

When used with a Pentek FMC carrier, Pentek's ReadyFlow® BSP provides control of all the 3324's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based FMC carrier IP modules as documented source code.

Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek FMC carrier IP with their own.

FMC Interface

The Model 3324 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3324 and the FMC carrier.

Model 3324 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J69
- **Sampling Rate:** up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel connectors

Transformer Type: Coil Craft WBC4-6TLB

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D and D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin Count FMC

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