

**WHAT WE DO****PCI-SYSTEMS**

manufactures a variety of COTS modular designed conduction cooled chassis for VPX and CPCI applications, including ATR and ARINC 600 enclosures.

**SWITCHED****BACKPLANE GEN.2**

NO STUB designs eliminate bandwidth degradation and allow RF signals to be connected via COAX connectors to the rear of the chassis. Switches are designed as mezzanine boards for small packaging and superior signal quality.

**3U extender for use in lab and development**

The VPX extender modules are built to extend a **3U VPX** module completely out of a chassis, providing access to all sides of the module for testing and debugging.

Or solution features a Tyco Multi-Gig RT-2 connector “**mini**” **backplane** to solve the problem of not having a right angle female connector.

The optional mezzanines are connected to the base board via **ERNI** high speed 10 **GBit/s** connectors.

Pin out: **Standard VPX 1 to 1**

- PCIe **Gen 3**
- Controlled impedance
- 100 Ohm differential pairs
- LED power rail status monitoring
- Conforms to VITA 46 VPX and OpenVPX
- Alignment keying provided on both sides of the extender
- Mechanical bracing available if needed

## Optional Mezzanines:

- Re-driver for add-on cards
- Re-driver for CPU slot
- Bus Analyzer 16 lane
- I/O



## Bus Analyzer Mezzanine

The 16 lane BusAnalyzer works in conjunction with PLX's on-chip diagnostic hardware, called visionPAK™. It enables designers to get to market faster with instant access to internal chip registers, and offers diagnostic features as well as performance monitoring of an entire system's performance, thus optimizing the usage of costly test equipment such as logic analyzers, traffic generators and high-speed oscilloscopes. Measuring the height and width quality of the SerDes eye, generating desired packets/traffic at line rate, injecting and counting errors, port utilization, and measuring performance are among the array of key features implemented in this BusAnalyzer. The ability to quickly debug systems in the lab while improving performance using the visionPAK™ Software, helps engineers to streamline their designs.

- New SerDes eye measurement enhancements includes SerDes height and width, plus gradient plot and time estimate
- Performance Monitor
- Packet Generator tool
- Special support for AHB register access
- Kernel drivers for PLX PCIe Gen 3 switches with on-chip DMA
- Compare register dump text files
- Slave Mode Loopback
- Auto-detection of Requestor ID for setting up Non-Transparent Mode Address Translation
- Java-based PEX Device Editor GUI for Linux

## WHAT WE DO

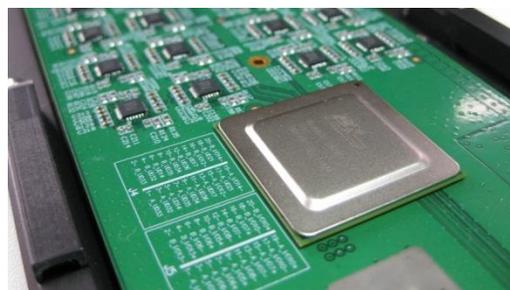
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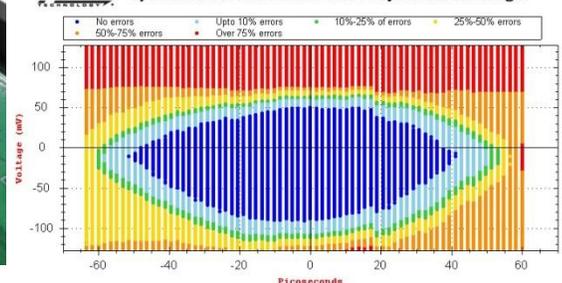
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**PLX** Special SDK Tool Measures SerDes Eye Width and Height



## ORDERING INFORMATION:

**Extender 3U VPX PCI\_300.500**  
**Redriver Mezzanine (P1) PCI\_300.501**  
**Passive Mezzanine (P2) PCI\_300.502**  
**Bus Analyzer 16 lane (P1) PCI\_300.503**