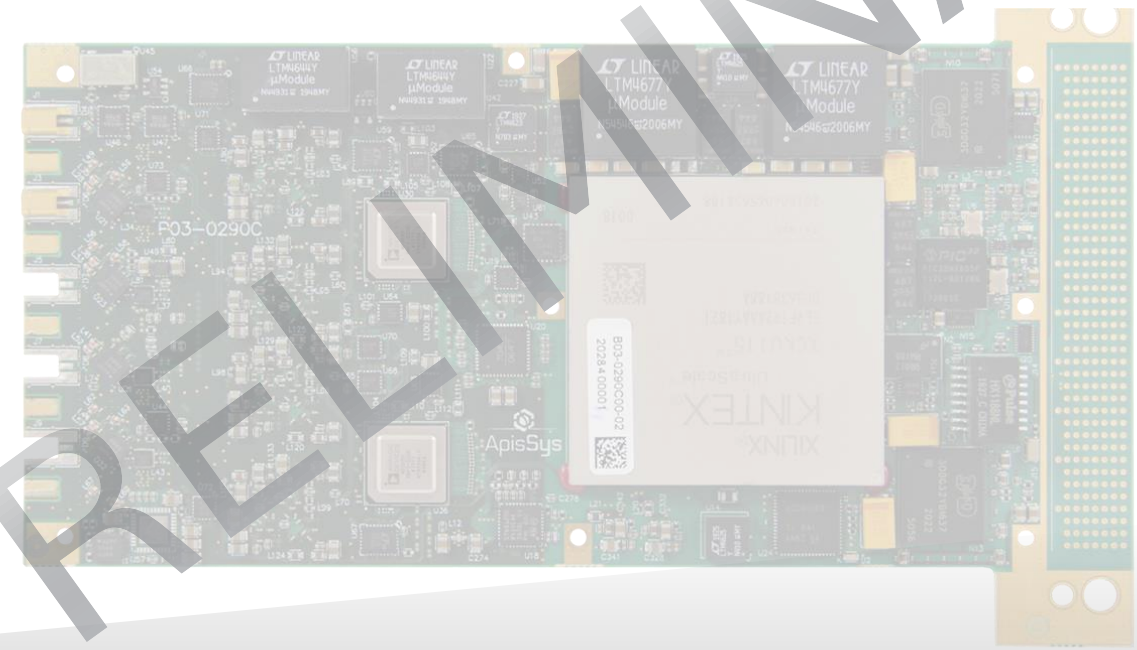
apissys
High tech
for innovators

AV 151

Phased-Array Radar Transceiver
EW-ESM/ECM

3U VPX / SOSA
Virtex UltraScale+ FPGA
Quad 12 bit 20 Gsps ADC
Quad 16 bit 28 Gsps DAC
Analog bandwidth up to 18GHz
Conduction Cooled



Applications

Phased-Array Radar Transmitter / Receiver
Electronic Warfare ESM /ECM
Broadband Communication

Features

4 channels 20 Gsps 12-bit ADC .
4 channels 28 Gsps 16-bit DAC .
Configurable DDC and DUC .
One Ultra Low jitter clock synthesizer .
External or internal sampling clock reference .
User programmable Xilinx® Virtex® Ultrascale+™ VU7P/VU9P/VU13P FPGA .
2x 64-bit 8GBytes DDR4 2666 SDRAM .
SOSA - aligned .
48x User-defined IO extension on P2 (optional)

SPECIFICATIONS

Form Factor

3U VPX Conduction cooled Vita 48.2, pitch 1.0”

VPX Profile

SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0
(SOSA-aligned)

Analog Input/Output

Input coupling: AC
Full power bandwidth: 100MHz to 18 GHz
Full scale: +2 dBm TBD
Output coupling: AC
Full power bandwidth: 100MHz to 14 GHz
Full scale: -4 dBm TBD
Impedance: 50 Ohm
Connectors: SMPM

Analog-Digital Conversion

Four channels, up to 20Gsps
Resolution: 12 bit
Configurable DUC and transmit FIR filter
Sampling Performances at 20Gsps
NSD: -164 dBFS/Hz at -3dBFS at 6GHz
HD2/HD3: -65dBFS at -7dBFS at 2GHz
IMD3: -75dBFS at -13dBFS at 2GHz

Digital-Analog Conversion

Four channels, up to 28Gsps
Resolution: 16 bit
Configurable DUC and transmit FIR filter
Sampling Performances @ 28Gsps
NSD: -164 dBFS/Hz at 0dBFS at 2GHz
IMD3: -75dBFS at -13dBFS at 2GHz to 10GHz

Clock

Ultra-low jitter clock synthesizers
External or internal sampling clock reference

Virtex Ultrascale+

XCVU7P-2FLVB104I
XCVU9P-2FLGB2104I
XCVU13P-2FHGB2104I

Memory

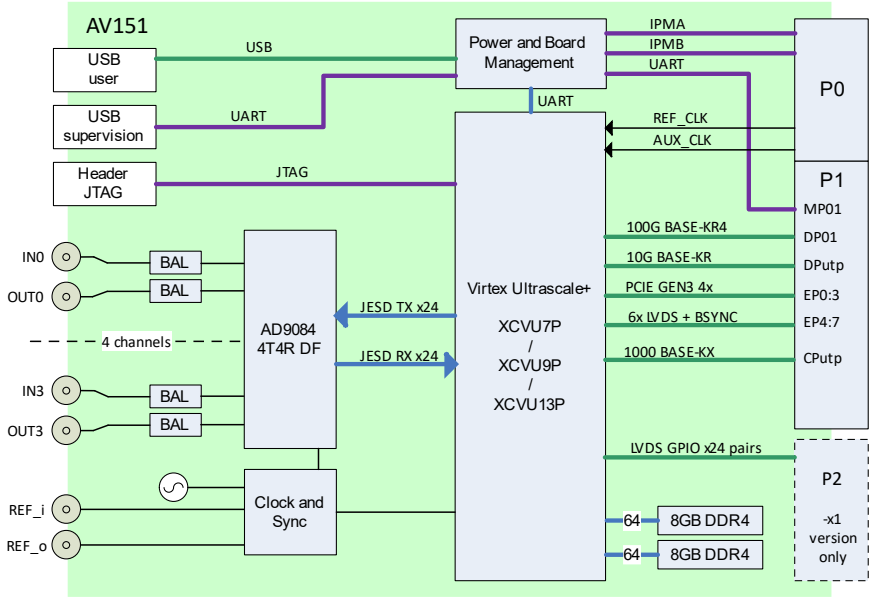
Two banks64-bit 8GBytes DDR4 266SDRAM
One 2 Gbit QSPI FLASH memory

Operating Temperature

Conduction cooled ECC3, -40°C to 70°C

Power dissipation

+12V: 14 A max (170W) TBD
+3.3VAUX: 0.6A max (2W) TBD



Weight

630g TBD

Board Support Package

FPGA + HPS exemple design
SW API and examples, Windows 10 64-bits / Linux 64-bits
User manuals
Quick start guide

VPX interface

P1:Data plane: one fat pipe DP01 supporting 100GBASE-KR4 -Data plane: one ultra-thin pipe DPutp01 supporting 10GBASE-KR -Control plane: one ultra-thin pipe CPutp01 supporting 1000BASE-KX. -Expansion plane: one fat-pipe supporting PCIE GEN3 4x -Expansion plane: 8 LVDS differential pairs, configurable as 16 single ended LVCMOS •

P2: -Empty (SOSA-aligned profile) or -24 LVDS differential pairs, configurable as 48 single ended LVCMOS

Environmental	Conduction-cooled Vita 47 class ECC3
Operating Temperature	-40°C to +70°C (Card Edge)
Non Operating Temperature	-50°C to +100°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.01g2 /Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing
Operating Attitude	@ -1,500 to 60,000 ft

Ordering informations

Part	Number	AV151	c	a	b
FPGA	FPGA Virtex Ultrascale+ VU7P		-	7	-
	FPGA Virtex Ultrascale+ VU9P		-	9	-
	FPGA Virtex Ultrascale+ VU13		-	13	-
VPX P2	Not fitted (SOSA-aligned)		-	-	0
	Fitted (48x User-defined IO extension)		-	-	1

CONTACT : sales@apissys.com

www.apissys.com