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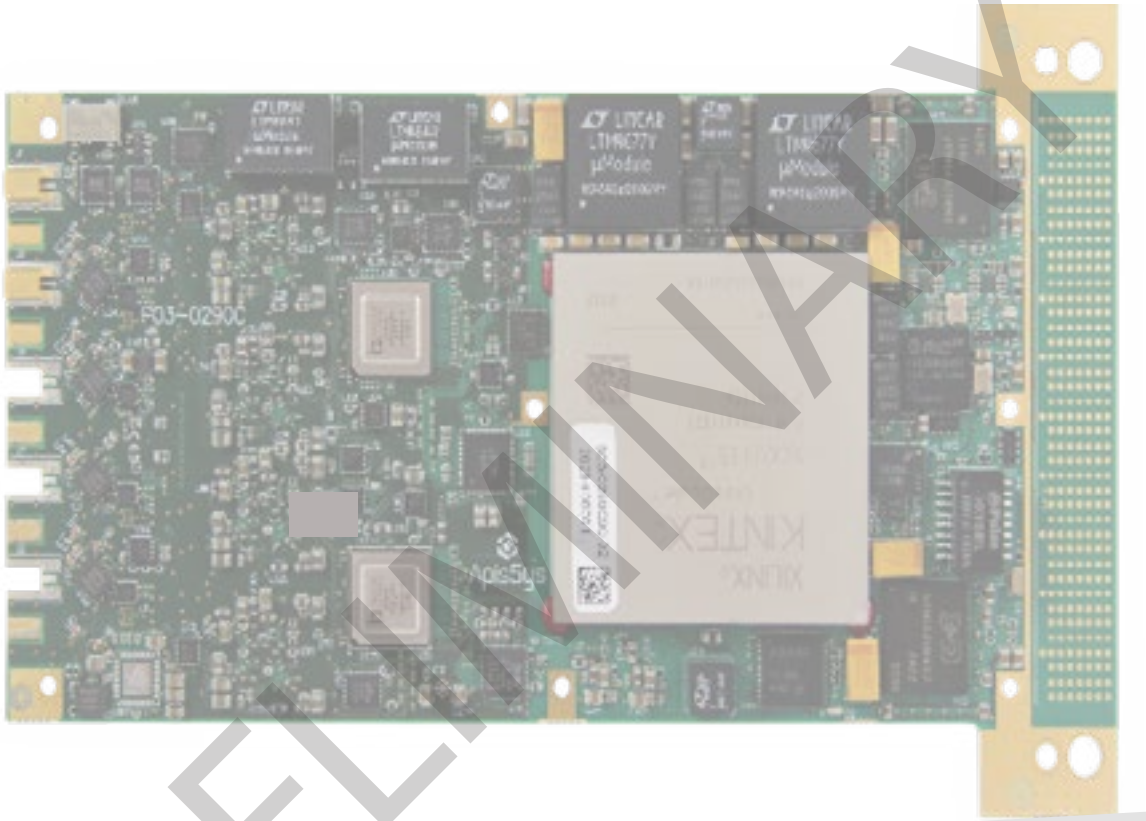
AV 150

Phased-Array Radar Transceiver
EW-ESM/ECM - MIMO

3U VPX
Virtex UltraScale+ FPGA
Quad 14 bit 3 Gsps ADC
Quad 16 bit 6 Gsps DAC
Conduction or Air-Cooled



Applications

· Phased-Array Radar Transmitter / Receiver
· Electronic Warfare ESM /ECM
· MIMO
· Wideband Communication

Features

· 4 channels 3 Gsps 14-bit ADC
. Independent Digital Down Converters, decimation factor 2 to 48.
· 4 channels 6/12 Gsps 16-bit DAC
· Independent Digital Up Converters, interpolation 2 to 24.
· One Ultra Low jitter clock synthesizers
· External or internal sampling clock
· External and internal sampling clock reference
· User programmable Xilinx® Virtex® Ultrascale+™ VU7P/VU9P/VU13P FPGA
· 2x 1G64 DDR4-2666 SDRAM
· 3U OpenVPX standard compliant
· Air cooled and Conduction cooled versions

Specifications

Analog Inputs/Outputs
- Input coupling: AC
- Full power bandwidth: > 10MHz to 8 GHz
- Full scale : 6 dBm TBD
- Output coupling: AC
- Full power 10MHz to 7.5 GHz
- Full scale : 0 dBm TBD
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion
- Four channels, Fs ≤ 3 GHz
- Resolution: 14 bit
- Sampling Performances @2.1 GHz -10dBFS
  - SNR: 55 dBFS @2.1 GHz
  - SFDR: 60 dBc @2.1 GHz
  - ENOB: 8.5 bit @2.1 GHz

Digital-Analog Conversion
- Four channels, Fs ≤ 6 GHz
- (12 GHz DAC update rate)
- Resolution: 16 bits
- Sampling Performances @2 GHz 5 Gsps
  - SFDR: 68 dBc (0dBFS)
  - NSD: -155 dBm/Hz

Clock
- Internal:
  - One ultra-low jitter clock synthesizers,
  - 2 GHz to 6 GHz low jitter clock
- External Input Clock:
  - Frequency: 10 MHz to 100 MHz
  - Input level: 10 dBm recommended
  - Connector: SMPM 50 Ohms
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

Digital Down Converter
- 2 independent DDC for each ADC:
  - Tuning frequency step: 48-bit NCO
  - DDC with 1/2 to 1/48 decimation ratio

Digital Up Converter
- 1 DUC for each DAC:
  - Tuning frequency step: 48-bit NCO
  - DUC with 2x to 24x interpolation ratio

FPGA
- FPGA: Xilinx Virtex Ultrascale+
  - XCVU7P-2FLVB2104I
  - XCVU9P-2FLGB2104I
  - XCVU13P-2FHGB2104I

Memory
- Two banks 1G64 DDR4 2666 SDRAM
- One 2 Gbit QSPI FLASH memory

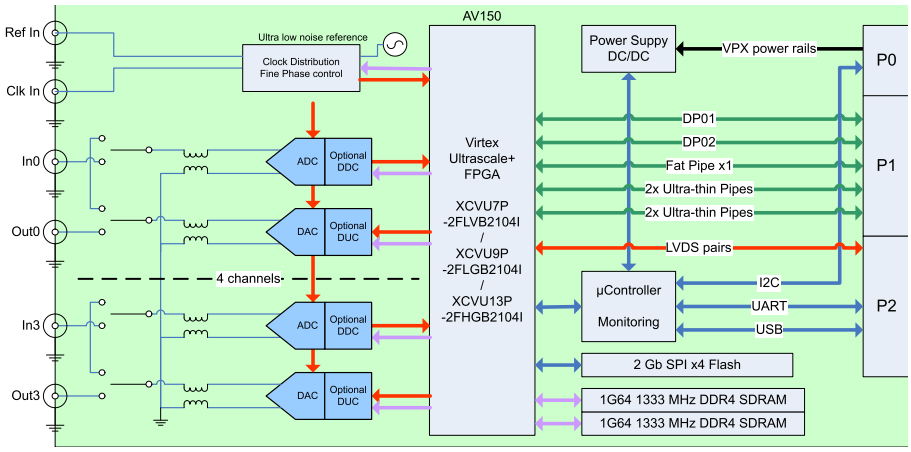
Software support
- Software Drivers:
  - Windows 10 64-bits
  - Linux 64-bits
- Application example: Windows and Linux

Firmware support
- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2022.2

Operating Temperature
Air-cooled EAC4, 0°C to 55°C
Conduction-cooled ECC3, -40°C to 70°C

Power dissipation (VU13P)
- +12V: 11.4 A max (137W) TBD
- +3.3VAUX: 0.6 A max (2W) TBD

Weight
- Air cooled : 550g TBD
- Conduction cooled : 650gTBD



VPX interface
- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and USB to UART
  - 24 LVDS differential pairs, configurable as 48 single ended LVCMOS

Environmental	Air-cooled Vita 47 class EAC4	Conduction-cooled Vita 47 class ECC3
Operating Temperature	0°C to 55C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.01g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing
Operating Attitude	0 to 10'000 ft with adequate airflow	-1,500 to 60,000 ft

Ordering information

Part	Number	AV150	c	a	b
Cooling	Air	-	A	-	-
	Conduction	-	C	-	-
FPGA	FPGA Virtex Ultrascale+ VU7P	-	-	7	-
	FPGA Virtex Ultrascale+ VU9P	-	-	9	-
	FPGA Virtex Ultrascale+ VU13P	-	-	13	-

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