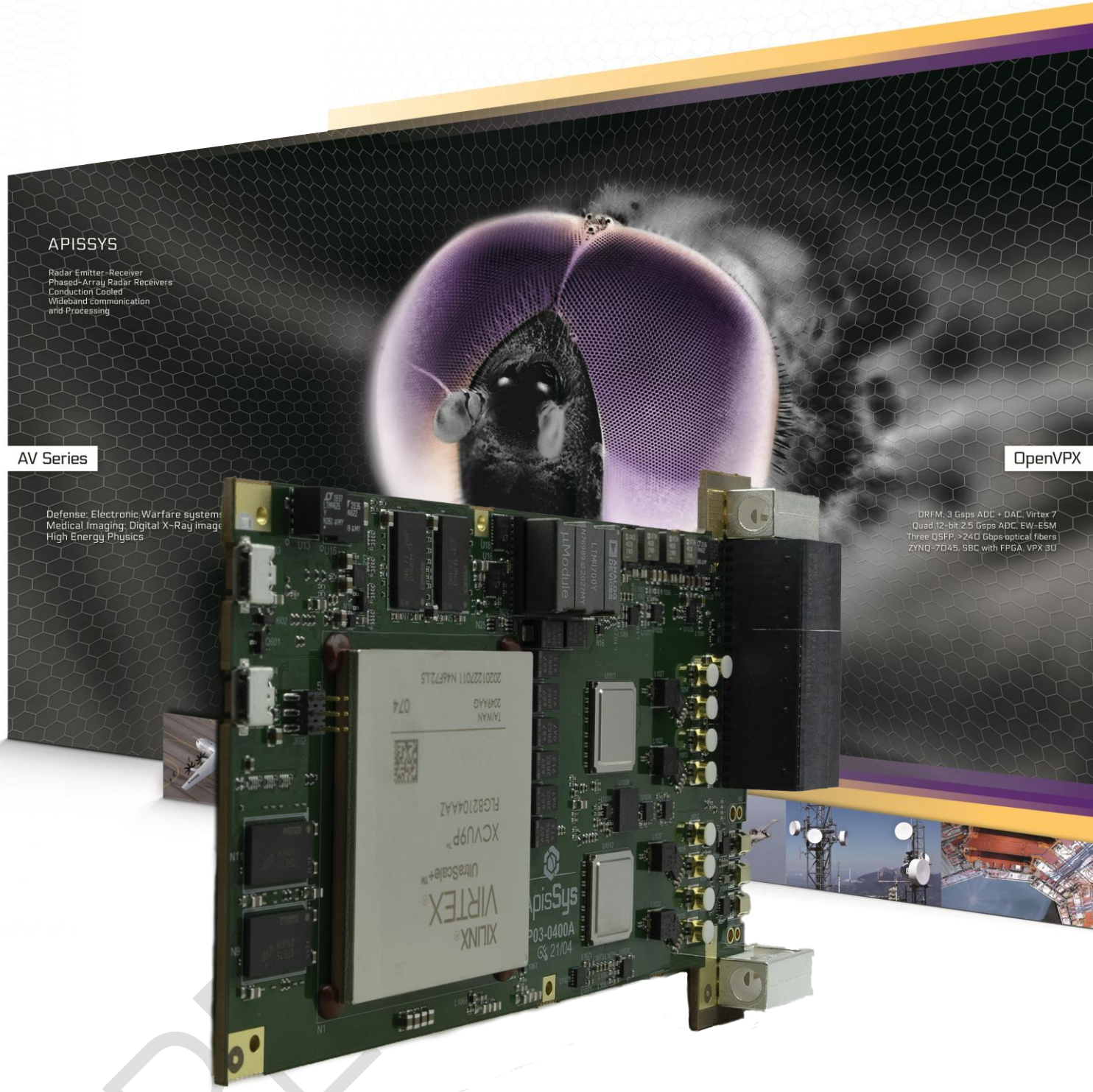


AV 140

Phased Array Radar Transceiver
EW-ESM - MIMO

- 3U VPX - SOSA Aligned
- Virtex UltraScale+ FPGA
- Quad 12-bit 6 Gsps ADC
- Quad 16-bit 12 Gsps DAC
- Conduction or Air-Cooled

ApisSys

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV140

Applications
- Electronic Warfare – Radar-ESM-RCM
- Wideband Radar Transmitter / Receiver
- Radar Target Generator
- MIMO
- Wideband Communication

Features
- 4 channels 6 Gsps 12-bit ADC
- 4 channels 12 Gsps 16-bit DAC
- One Ultra Low jitter clock synthesizer
- External or internal sampling clock
- External or internal sampling clock reference
- User programmable Xilinx® Virtex® Ultrascale+™ VU9P/VU13P FPGA
- 2x 1G64 DDR4-2666 SDRAM
- 3U OpenVPX standard compliant – SOSA Aligned
- Air cooled and Conduction cooled rugged versions

Overview

The AV140 is part of ApisSys' range of High-Speed data conversion and signal processing solutions based on the VITA 46, VPX standard. The AV140 is SOSA aligned with RF signals on the backplane according to VITA 67.3 standard.

The AV140 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, and up to 40 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.

The AV140 combines four channel 12-bit 6 Gsps ADC and four channels 16-bit 12 Gsps DAC with ultra-high processing power delivered by Xilinx® Virtex® Ultrascale+™ FPGA, making it ideally suited for embedded signal processing applications such as Electronic Warfare, Wideband Radar Transmitter/Receivers or Wideband Communication applications.

The AV140 features an internal ultra-low jitter reference and one clock synthesizer and can be used with either external clock or external reference for higher flexibility.

The AV140 includes one Xilinx® Virtex® Ultrascale+™ VU13P FPGA for an impressive processing capability of more than 19 TMACs (Multiply Accumulate per second), two 1G64 DDR4-2666 SDRAM memory for data processing and one 2 Gb synchronous FLASH memory for multiple firmware storage. The AV140 can also be fitted with one Xilinx® Virtex® Ultrascale+™ VU9P FPGA.

The AV140 provides a UART and a USB 2.0 interfaces intended to be used for system monitoring and supervision.

The AV140 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

12-bit 6 Gsps ADCs

The AV140 Analog to Digital conversion is performed by two Analog Devices AD9082 Mixed Signal Front Ends (MxFE®) dual-channel 12-bit 6 Gsps ADC

The AV140 provides four SMPM for analog inputs on the 14-port VITA 67.3 connector.

Single ended input signals are AC coupled with a usable input bandwidth from 10 MHz to more than 8 GHz with (TBD) dBm input level.

16-bit 12 Gsps DACs

The AV140 Digital to Analog conversion is performed by two Analog Devices AD9082 Mixed Signal Front Ends (MxFE®) dual-channel 16-bit 12 Gsps DAC.

The AV140 provides four SMPM for analog outputs on a 14-port VITA 67.3 connector.

Single ended output signals are AC coupled with a usable ouput bandwidth from 10 MHz to more than 8 GHz with (TBD) dBm output level (NRZ).

Clock

The AV140 provides one ultra-low jitter clock synthesizer locked on a 100 MHz internal reference.

The AV140 supports a 10 to 500 MHz external reference input from a SMPM on the 14-port VITA 67.3 connector. A reference output is available on the VITA 67.3 connector.

An external sampling clock input from 4 GHz to 12 GHz is supported from one SMPM on the 14-port VITA 67.3 connector.

Calibration

A wideband signal generator plus internal Loopback from the DAC output allow for stand-alone calibration of all ADC and DAC channels. External input and output calibration signals are supported on the 14-port VITA 67.3 connector.

FPGA

The AV140 is fitted with a Xilinx® Virtex® Ultrascale+™ VU9P or VU13P user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR4 SDRAM and monitoring sub-system, leaving most of the logic and block RAM and all DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex Ultrascale+ VU13P FPGA includes 3,780 K logics cells, 94.5 Mbit of RAM blocs, 360 Mbit of Ultra RAM, 4 PCIe GEN3x16 interface blocs and 12,288 DSP48 slices for an impressive processing power of more than 19 TMACs.

The FPGA is delivered in -2 speed grade.

Memories

The AV140 includes two 512M64 (1G64) DDR4-2666 SDRAM memory banks and one 2 Gbit QSPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV140 features an OpenVPX VITA 65 compliant interface, SOSA aligned, with support for one Fat Pipe and one Ultra-Thin Pipe for Data Planes, one Ultra-Thin Pipe for Control Plane and two Fat Pipes for Expansion Plane on P1.

The AV140 features one low phase noise clock generator able to synthesize the clock references for the FPGA GTYs from 60 MHz to 820 MHz, allowing support of all major protocols such as Aurora, 10 and 40GigE, PCIe Gen 1, 2 and 3, SATA, SRIO and 1Gbit Ethernet up to 28 Gbps.

Microcontroller

The AV140 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.

The microcontroller supports a USB 2.0 and a UART interfaces accessible on the front panel.

The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware

The AV140 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV140 hardware resources.

A base design is provided which demonstrates the use of the AV140 and gives users a starting point for firmware development. The AV140 firmware package is supported on the Xilinx VIVADO® 2019.1 design suite and later.

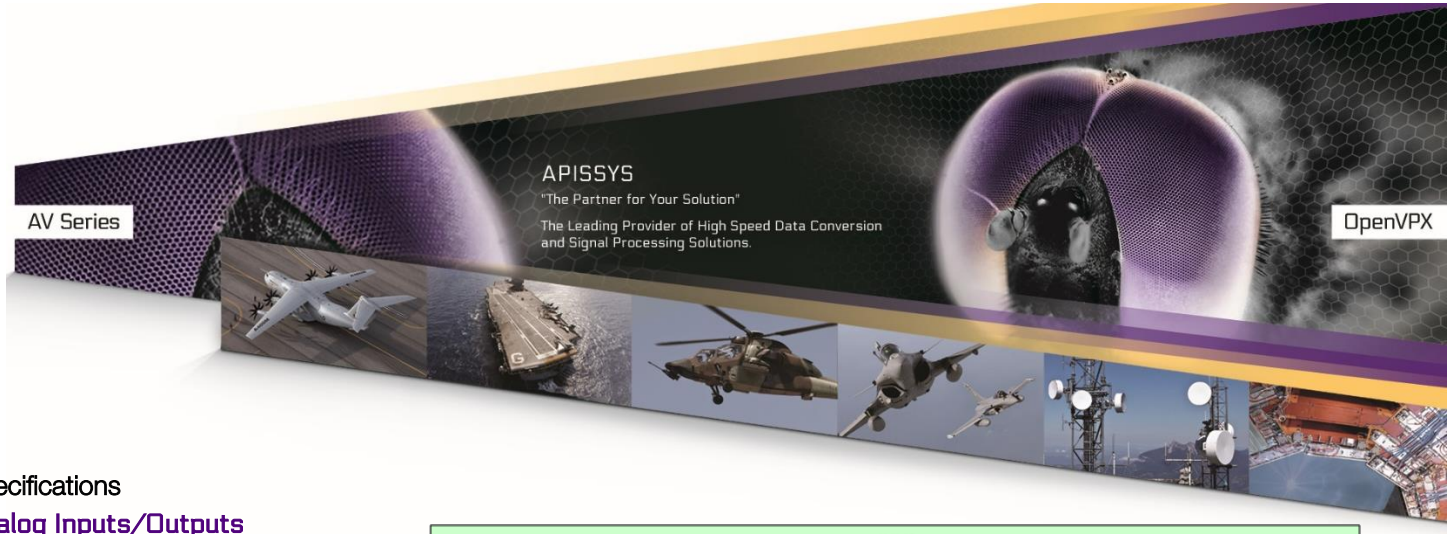
Software

The AV140 is delivered with software drivers for Windows 10 and Linux.

Ruggedization

The AV140 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.



Specifications

Analog Inputs/Outputs

- Input coupling: AC
  - Full power bandwidth: > 8 GHz
  - Full scale : TBD dBm
- Output coupling: AC
  - Full power bandwidth: > 8 GHz
  - Full scale : TBD dBm (NRZ)
- Impedance: 50 Ohm
- Connectors: SMPM on VITA 67.3

Analog-Digital Conversion

- Four channels, Fs ≤ 6 GHz /
- Resolution: 12 bit
- Sampling Performances @2.1 GHz -1dBFS
  - SNR: 54 dBFS
  - SFDR: 70 dBc
  - ENOB: 8.6 bit

Digital-Analog Conversion

- One channel, Fs ≤ 12 GHz
- Resolution: 16 bit
- Sampling Performances @2.1 GHz, -7 dBFS
  - SFDR: 68 dBc
  - NSD: -160 dBc/Hz

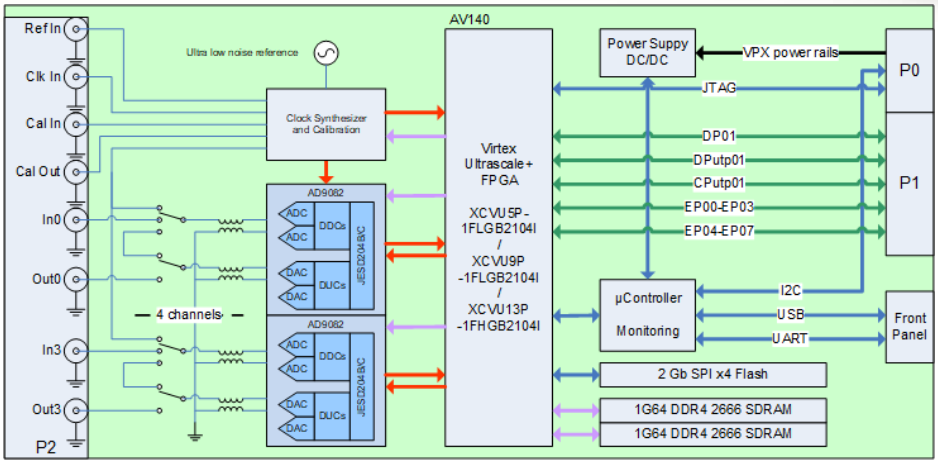
Clock

- Internal:
  - One ultra-low jitter clock synthesizers,
  - 4 GHz to 12 GHz low jitter clock
- External Input Clock:
  - Frequency: 4 GHz to 12 GHz
  - Input level: 10 dBm recommended
  - Connector: SMPM 50 Ohms on VITA 67.3
- External reference:
  - frequency: 10 MHz to 500 MHz
  - Connector: SMPM, 50 Ohm on VITA 67.3

Calibration

- One low jitter signal generator
  - Frequency: 1 GHz to 4.5 GHz
- External Calibration input and output:

Connectors: SMPM, 50 Ohm on VITA 67.3



FPGA

- FPGA: Xilinx Virtex Ultrascale+
  - XCVU13P-2FHGB2104I
  - XCVU9P-2FLBG2104I

Memory

- Two banks 512M64 DDR4 SDRAM, 1333 MHz clock
  - Support up to two banks 1G64 DDR4 SDRAM
- One 2 Gbit QSPI FLASH memory

VPX interface

- P1:
  - Data plane: one fat pipe and one ultra-thin pipe
  - Control plane: one ultra-thin pipe
  - Expansion plane: two fat pipes
- P2:
  - VITA 67.3 14-port

Software support

- Software Drivers:
  - Windows 10 64-bits
  - Linux 64-bits
- Application example: Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2019.1 and later

Ruggedization

- As per VITA 47:
  - Air cooled: EAC4 and EAC6
  - Conduction cooled: ECC3 and ECC4

Power dissipation (VU13P)

- +12V: 11.9 A max (143W)
- +3.3VAUX: 0.6 A max (2W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ordering information

Part Number		AV140	–	rr	–	a
Ruggedization level	Air Standard	-	-	AS	-	-
	Air Rugged	-	-	AR	-	-
	Conduction Standard	-	-	CS	-	-
	Conduction Rugged	-	-	CR	-	-
Options 1	FPGA Virtex Ultrascale+ VU9P	-	-	-	-	1
	FPGA Virtex Ultrascale+ VU13P	-	-	-	-	2

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

Reference to ANSI-VITA standard 47 for the listed parameters only.

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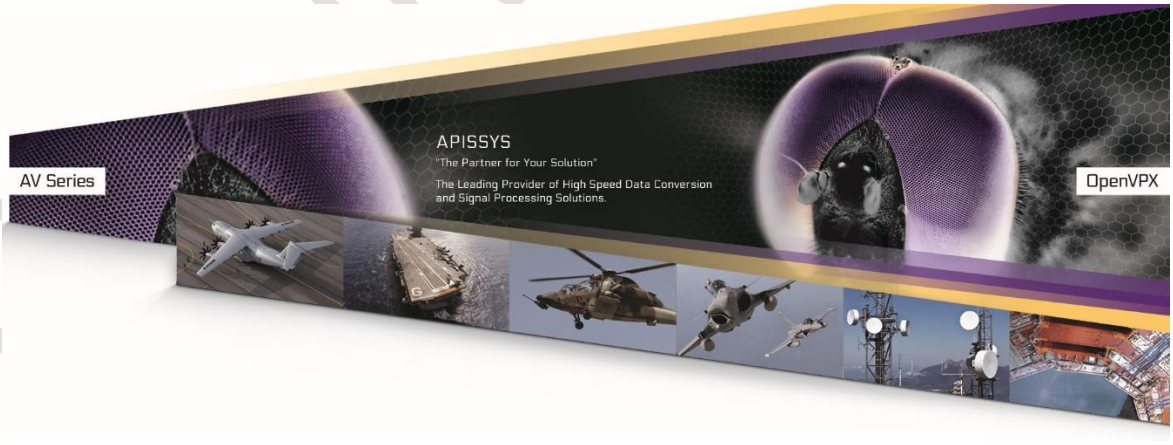

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