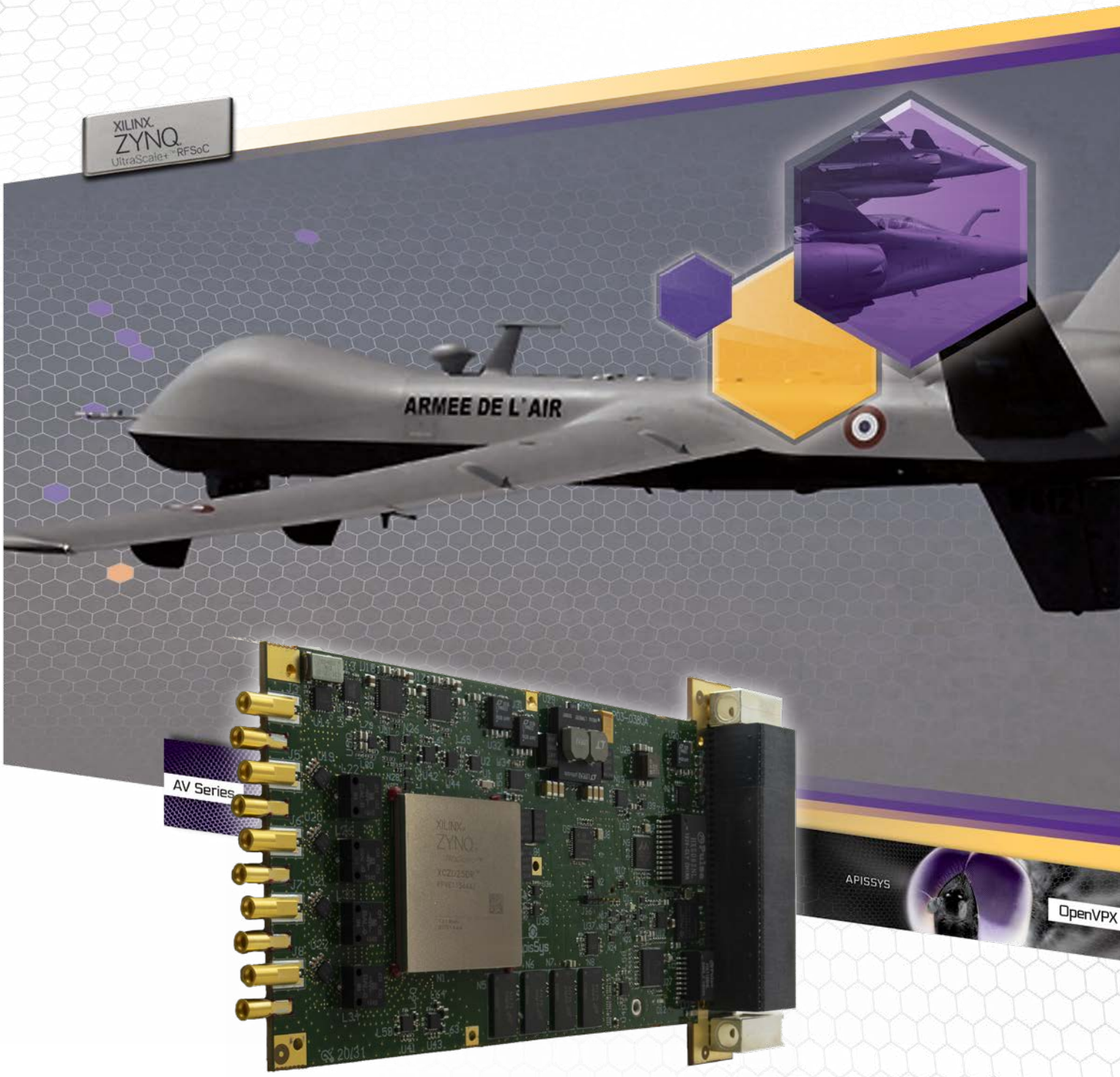


AV 138

Phased Array Radar Transceiver
EW-ESM/ECM - MIMO

3U VPX
ZYNQ UltraScale+ RFSoC
Quad 12-bit 4 Gsps / 14-bit 5 Gsps ADC
Quad 14-bit 6 Gsps / 14-bit 10 Gsps DAC
Conduction or Air-Cooled

ApisSys

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV 138

Applications
· Electronic Warfare – Radar-ESM - ECM
· Wideband Radar Transmitter / Receiver
· MIMO
· Wideband Communication

Features
· 4 channels 12-bit 4 Gsps / 14-bit 5 Gsps ADC
· 4 channels 14-bit 6 Gsps / 14-bit 10 Gsps DAC
· Two Ultra Low jitter clock synthesizers
· External or internal sampling clock reference
· User programmable Xilinx® ZYNQ® Ultrascale+™ ZU25DR / ZU27DR / ZU47DR RFSoC
· One bank up to 1G64 DDR4-2400 SDRAM
· One 1TB NVMe embedded SSD.
· 3U OpenVPX standard compliant
· Air cooled and Conduction cooled rugged versions

Overview
The AV138 is part of ApisSys' range of High-Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.
The AV138 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.
The AV138 includes one Xilinx® ZYNQ® Ultrascale+™ RFSoC, GEN 1 XCZU25DR or XCZU27DR or GEN 3 XCZU47DR with the minimum external resources for low power applications.
The AV138 features four channels 12-bit 4.096 Gsps ADC and four channels 14-bit 6.554 Gsps DAC or four channel 14-bit 5 Gsps ADC and four channels 14-bit 10 Gsps DAC with optimized analog performances, making it ideally suited for embedded signal processing applications such as Electronic Warfare, Wideband Radar Transmitter/Receivers or Wideband Communication applications.
The AV138 features one internal ultra-low jitter reference and two clock synthesizers and can be used with external reference for higher flexibility.
The AV138 Xilinx® ZYNQ® Ultrascale+™ RFSoC XCZU27DR or XCZU47DR provides an impressive processing capability of more than 5.5 TMACs (Multiply Accumulate per second), four 1333 MHz Arm Cortex-A53 cores, one 512M64 or 1G64 DDR4-2400 SDRAM memory for data processing, two 2 Gb synchronous FLASH memory for program boot and one 1TB NVMe embedded SSD. The AV138 can also be fitted with one Xilinx® ZYNQ® Ultrascale+™ XCZU25DR.
The AV138 provides one GbE, one UART and one USB 2.0 interfaces.

14-bit 5 Gsps ADCs
The AV138 supports four Analog to Digital conversion channels from the RFSoC with up to 14-bit 5 Gsps conversion rate on the GEN 3 device and 12-bit 4.096 Gsps on the GEN 1 devices.
The AV138 provides four front panel SMPM connectors for analog inputs.
Single ended input signals are AC coupled with an input bandwidth from 1 MHz to more than 6 GHz with 10 dBm input level.
Internal Loopback from the DAC outputs allows for stand-alone calibration.

14-bit 10 Gsps DACs
The AV138 supports four Digital to Analog conversion channels from the RFSoC with up to 14-bit 10 Gsps conversion rate on the GEN 3 device and 14-bit 6.554 Gsps on the GEN 1 devices.
The AV138 provides four front panel SMPM connectors for analog outputs.
Single ended output signals are AC coupled with an ouput bandwidth from 1 MHz to more than 6 GHz with -8 dBm output level.

Clock
The AV138 provides one ultra-low jitter clock synthesizer for the ADC channels and one ultra-low jitter clock synthesizer for the DAC channels, both locked on a common 100 MHz internal reference or on the external reference.
The AV138 supports a 10 to 200 MHz external reference input either from a front panel SMPM connector or from the VPX P2 Connector. A reference output is available on a front panel SMPM connector and on VPX P2.

RFSoC
The AV138 is fitted with a Xilinx® ZYNQ® Ultrascale+™ GEN1 XCZU25DR, XCZU27DR or GEN3 XCZU47DR user programmable RFSoC. Only few resources are used to control and communicate with external hardware such as VPX Interface or clock synthesizers, leaving most of the logic, block RAM, Ultra RAM and all DSP resources available for customer processing.
Dedicated to signal processing, the Xilinx ZYNQ Ultrascale+ XCZU27DR or XCZU47DR RFSoC include 930 K logics cells, 38 Mbit of RAM blocs, 22.5 Mbit of Ultra RAM, 2 PCIe GEN3x16 interface blocs and 4,272 DSP48 slices for an impressive processing power of more than 5.5 TMACs.
The RFSoC is delivered in -2 speed grade.

VPX interface
The AV138 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane connected to the RFSoC Programmable Logic.
The AV138 also supports one GbE interface configurable as 1000BASE-T or 1000BASE-BX, one UART and one USB2.0 interfaces connected to the RFSoC Processing System.
The AV138 features 18 LVDS differential pairs configurable as 36 single-ended LVCMOS on P2.
The AV138 features one low phase noise clock generator able to synthesize clock references for the RFSoC GTRs and GTYs, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1, 2 and 3, SATA, SRIO and XAUI 10Gbit Ethernet up to 25.785 Gbps.

Memories
The AV138 includes one 512M64, with support for up to 1G64, DDR4-2400 SDRAM memory bank connected to the RFSoC Processing System.
The AV138 features two 2 Gbit QSPI FLASH memories used to store the RFSoC boot files and Programmable Logic configuration files.
A 512GB or 1TB NVMe SSD is connected to the RFSoC Processing System embedded PCIe interface for data storage.

Software and Firmware
The AV138 is delivered with a Linux distribution for the Arm Cortex-A53 cores.
The AV138 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV138 hardware resources.
A base design is provided which demonstrates the use of the AV138 and gives users a starting point for firmware development. The AV138 firmware package is supported on the Xilinx VIVADO® 2019.1 design suite.

Software
The AV138 is delivered with a Linux BSP.

Ruggedization
The AV138 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC4, EAC6 and ECC4.

Specifications

Analog Input/Output

- Input coupling: AC
  - Full power bandwidth: > 3.5 GHz (GEN1)
  - Full power bandwidth: > 6 GHz (GEN3)
  - Full scale : 10 dBm
- Output coupling: AC
  - Full power bandwith: > 4 GHZ (GEN1)
  - Full power bandwidth: > 6 GHz (GEN3)
  - Full scale : -8 dBm
- Impedance: 50 Ohm
- Connectors: SMPM
- Analog-Digital Conversion

Analog-Digital Conversion

- GEN 3:
  - four channels, 14-bit Fs ≤ 5 GHz
  - NSD: -144 dBFS/Hz
  - SFDR: 80 dBc (TBC, excl. H2 and H3)
- GEN 1:
  - four channels, 12-bit Fs ≤ 4.096 GHz
  - NSD: -150 dBFS/Hz
  - SFDR: >73 dBc (excl. H2 and H3)

Digital-Analog Conversion

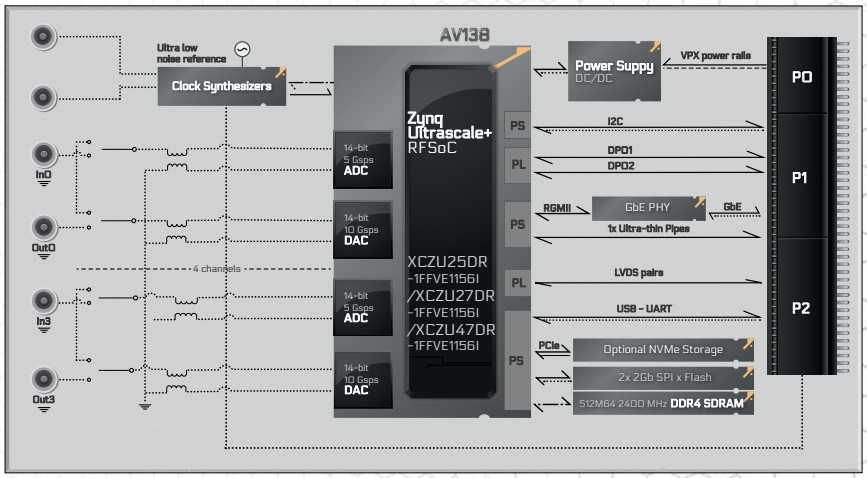
- GEN 3:
  - four channels, 14-bit Fs ≤ 10 GHz
  - NSD: -155 dBm/Hz
  - SFDR: 80 dBc (TBC, excl. H2, H3 and Fs/2)
- GEN 1:
  - four channels, 14-bit Fs ≤ 6.554 GHz
  - NSD: -145 dBm/Hz
  - SFDR: > 67 dBc (excl. H2, H3 and Fs/2)

Clock

- Internal:
  - One 100 MHz ultra-low phase noise clock reference
  - Two ultra-low jitter clock synthesizers, 500 MHz to 10 GHz.
- External reference:
  - frequency: 10 MHz to 200 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

Xilinx ZYNQ Ultrascale+ RFSoC

- XCZU25DR- 1FFVE1156I
- XCZU27DR- 1FFVE1156I
- XCZU47DR- 1FFVE1156I



Memory

- One bank 512M64 DDR4 SDRAM, 1200 MHz clock
  - Support up to one bank 1G64 DDR4 SDRAM
- Two 2 Gbit QSPI FLASH memory
- One 512 GB or 1 TB NVMe SSD on PCIe GEN2 x2

VPX interface

- P1:
  - Data plane: two fat pipes
  - Control plane: one ultra-thin pipes for 1000BASE-BX
  - one thin pipe for 1000BASE-T
  - User-defined ultra-thin pipes: UART and USB2.0.
- P2:
  - 18 LVDS differential pairs, configurable as 36 LVCMOS

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2019.2

Software support

- Software:
  - Linux 64-bits for Arm Cortex-A53 cores

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC4

Power dissipation (ZU47DR)

- +12V: 4 A max (48W)
- +5V: 0 A max (0W)
- +3.3V: 0 A max (0W)
- +3.3VAUX: 0.2 A max (1W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ordering information

Part Number		AV138	-	rr	-	a
Ruggedization level	Air Standard	-	-	AS	-	-
	Air Rugged	-	-	AR	-	-
	Conduction Rugged	-	-	CR	-	-
Options 1	ZYNQ Ultrascale+ RFSoC ZU25DR	-	-	-	-	1
	ZYNQ Ultrascale+ RFSoC ZU27DR	-	-	-	-	2
	ZYNQ Ultrascale+ RFSoC ZU47DR	-	-	-	-	3

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 60,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

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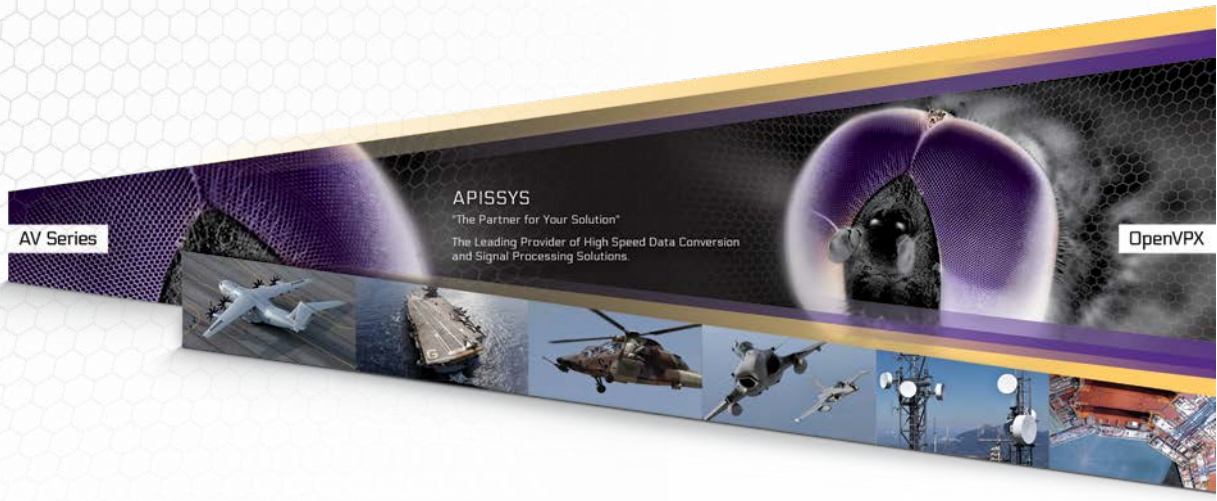
Design By vert-pomme.ch - 01.2016



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