AV 133

Wideband Radar Transceiver
EW-ECM – DRFM

3U VPX
Virtex Ultrascale+ FPGA
12 bit 5.4 Gsps ADC – DAC
Conduction or Air-Cooled

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV 133

Applications

- Electronic Warfare – Electronic Attack
- DRFM
- Radar Transmitter / Receiver
- Radar Target Simulator
- Wideband Communication

Features

- 1 channel 5.4 Gsps 12-bit ADC
- 1 channel 5.4 Gsps 12-bit DAC
- One Ultra Low jitter clock synthesizers
- External or internal sampling clock
- External and internal sampling clock reference
- User programmable Xilinx® Virtex® Ultrascale+™ VU9P/VU13P FPGA
- 2x 1G64 DDR4-2666 SDRAM
- 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions

Overview

The AV133 is part of ApisSys' range of High-Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.
The AV133 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.
The AV133 combines one channel 12-bit 5.4 Gsps ADC and one channel 12-bit 5.4 Gsps DAC with ultra-high processing power delivered by Xilinx® Virtex® Ultrascale+™ FPGA, making it ideally suited for embedded signal processing applications such as Electronic Warfare, Wideband Radar Transmit¬ter/Receivers or Wideband Communication applications.
The AV133 features an internal ultra-low jitter reference and one clock synthesizer and can be used with either external clock or external reference for higher flexibility.
The AV133 includes one Xilinx® Virtex® Ultrascale+™ VU13P FPGA for an impressive processing capability of more than 19 TMACs (Multiply Accumulate per second), two 1G64 DDR4-2666 SDRAM memory for data processing and one 2 Gb synchronous FLASH memory for multiple firmware storage. The AV133 can also be fitted with one Xilinx® Virtex® Ultrascale+™ VU9P FPGA.
The AV133 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.
The AV133 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

12-bit 5.4 Gsps ADC

The AV133 Analog to Digital conversion is performed by one e2v EV12AS350 12-bit 5.4 Gsps ADC.
The AV133 provides one front panel SMPM connector for analog input.
Single ended input signal is AC coupled with an input bandwidth from 1 MHz to more than 5.5 GHz with 8.5 dBm input level.

12-bit 5.4 Gsps DAC

The AV133 Digital to Analog conversion is performed by one e2v EV12DS460 12-bit 6 Gsps DAC.
The AV133 provides one front panel SMPM connector for analog output.
Single ended output signal is AC coupled with an output bandwidth from 1 MHz to more than 6 GHz with -3.5 dBm output level (NRZ).

Clock

The AV133 provides one ultra-low jitter clock synthesizers locked on a 100 MHz internal reference. The AV133 supports a 10 to 100 MHz external reference input either from a front panel SMPM connector or from the VPX P2 Connector. A reference output is available on VPX P2. External clock inputs for the ADC and DAC is supported from either one SMPM connector or VPX P2. External clock from 2 GHz to 5.4 GHz are supported. External clock outputs are provided on an SMPM connector and on VPX P2.

Trigger and Synchronization

The AV133 provides one front panel SMPM connector for external trigger input and one SMPM connector for a trigger output.

FPGA

The AV133 is fitted with a Xilinx® Virtex® Ultrascale+™ VU9P or VU13P user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR4 SDRAM and monitoring sub-system, leaving most of the logic and block RAM and all DSP resources available for customer processing. Dedicated to signal processing, the Xilinx Virtex Ultrascale+ VU13P FPGA includes 3,780 K logics cells, 94.5 Mbit of RAM blocs, 360 Mbit of Ultra RAM, 4 PCIe GEN3x16 interface blocs and 12,288 DSP48 slices for an impressive processing power of more than 19 TMACs.
The FPGA is delivered in -2 speed grade.

Memories

The AV133 includes two 512M64 (1G64) DDR4-2666 SDRAM memory banks and one 2 Gbit QSPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV133 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra-Thin Pipes for Control Plane and two User Defined Ultra-Thin Pipes on P1. The AV133 also supports 18 LVDS differential pairs configurable as 36 single-ended LVCMOS on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.
The AV133 features two low phase noise clock generators able to synthesize clock references for the FPGA GTHs from 60 MHz to 820 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1, 2 and 3, SATA, SRIO and XAUI 10Gbit Ethernet up to 28 Gbps.

Microcontroller

The AV133 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.
The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board. The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware

The AV133 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV133 hardware resources.
A base design is provided which demonstrates the use of the AV133 and gives users a starting point for firmware development. The AV133 firmware package is supported on the Xilinx VIVADO® 2019.2 design suite.

Software

The AV133 is delivered with software drivers for Windows 10 and Linux.

Ruggedization

The AV133 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.

Specifications

Analog Input/Output

- Coupling: AC
- Input bandwidth: > 5.5 GHz
- Input Full scale : 8.5 dBm
- Output bandwidth: > 6 GHz
- Output Full scale : -3.5 dBm (NRZ)
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion

- One channel, Fs ≤ 5.4 GHz
- Resolution: 12 bit
- Analog Performances @1 GHz, -1dBFS
  - SNR: 53 dBFS
  - SFDR: 56 dBc
  - ENOB: 8.5 bit

Digital-Analog Conversion

- One channel, Fs ≤ 5.4 GHz
- Resolution: 12 bit
- Analog Performances @1 GHz, 0dBFS
  - SFDR: 59 dBc, NRTZ mode
- Analog Performances @3 GHz, 0dBFS
  - SFDR: 55 dBc, NRTZ mode

Clock

- Internal:
  - 1 GHz to 6 GHz low jitter clock
- External Input Clock:
  - Frequency: 2 GHz to 5.4 GHz
  - Input level: 10dBm recommended
  - Connector : SMPM 50 Ohm and VPX P2
- External reference:
  - Frequency: 10 MHz to 100 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

Trigger

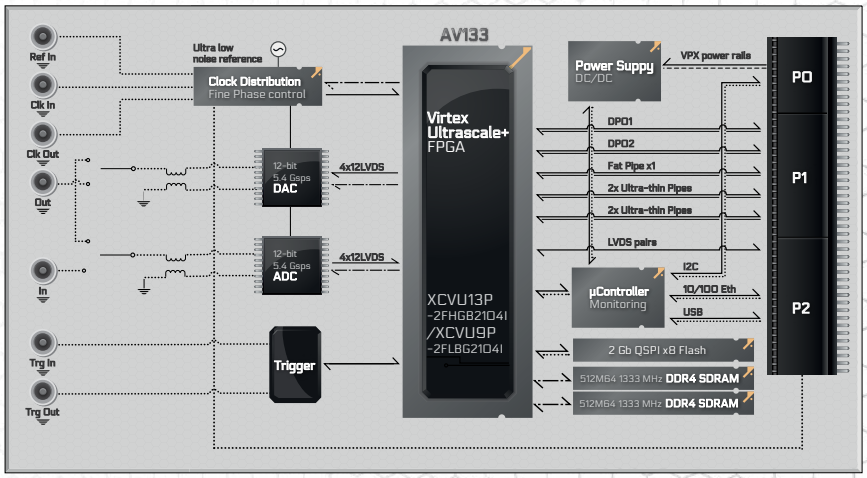
- External: 0 to 2 Vp
- Connectors: SMPM, 50 Ohm:

FPGA

- FPGA: Xilinx Virtex Ultrascale+
  - • XCVU13P-2FHGB2104I
  - • XCVU9P-2FLBG2104I

Memory

- Two banks 512G64 DDR4 SDRAM, 1333 MHz clock



- Support up to two banks 1G64 DDR4 SDRAM
- One 2 Gbit QSPI FLASH memory

VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 18 LVDS differential pairs, configurable as 36 LVCMOS

Software support

- Software Drivers:
  - Windows 10 64 bits
  - Linux 64 bits
- Application example: Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2019.2

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

Power dissipation

- +12V: 9.7 A max (116W)
- +5V: 2.4 A max (12W)
- +3.3V: 2.0 A max (6.5W)
- +3.3VAUX: 0.6 A max (2.0W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ordering information

Part Number		AV133	-	rr	-	a
Ruggedization level	Air Standard	-	-	AS	-	-
	Air Rugged	-	-	AR	-	-
	Conduction Standard	-	-	CS	-	-
	Conduction Rugged (contact factory)	-	-	CR	-	-
Options 1	FPGA Virtex Ultrascale+ VU9P	-	-	-	-	1
	FPGA Virtex Ultrascale+ VU13P	-	-	-	-	2

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 60,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

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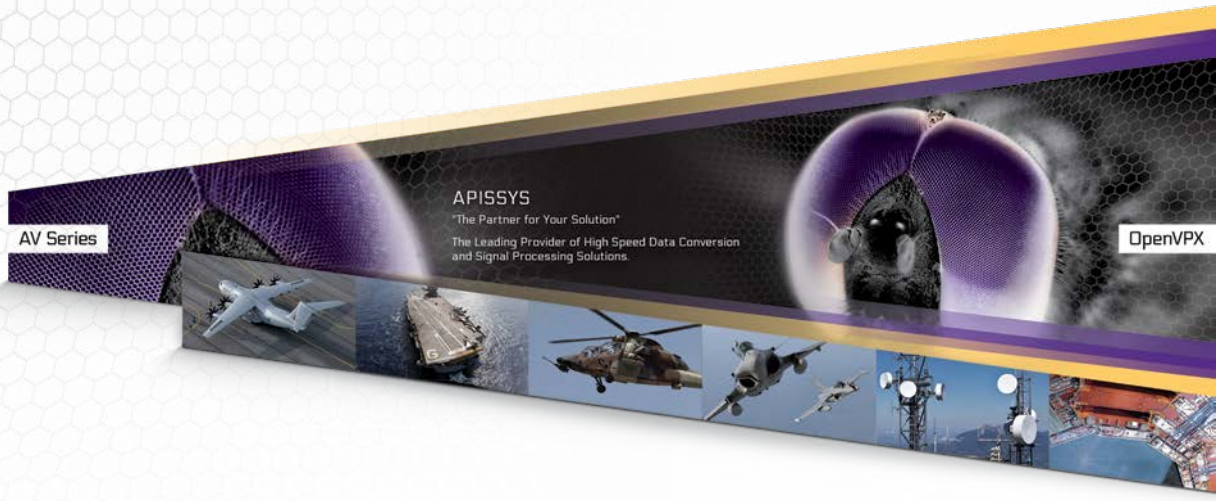
Design By vert-pomme.ch - 01.2016



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