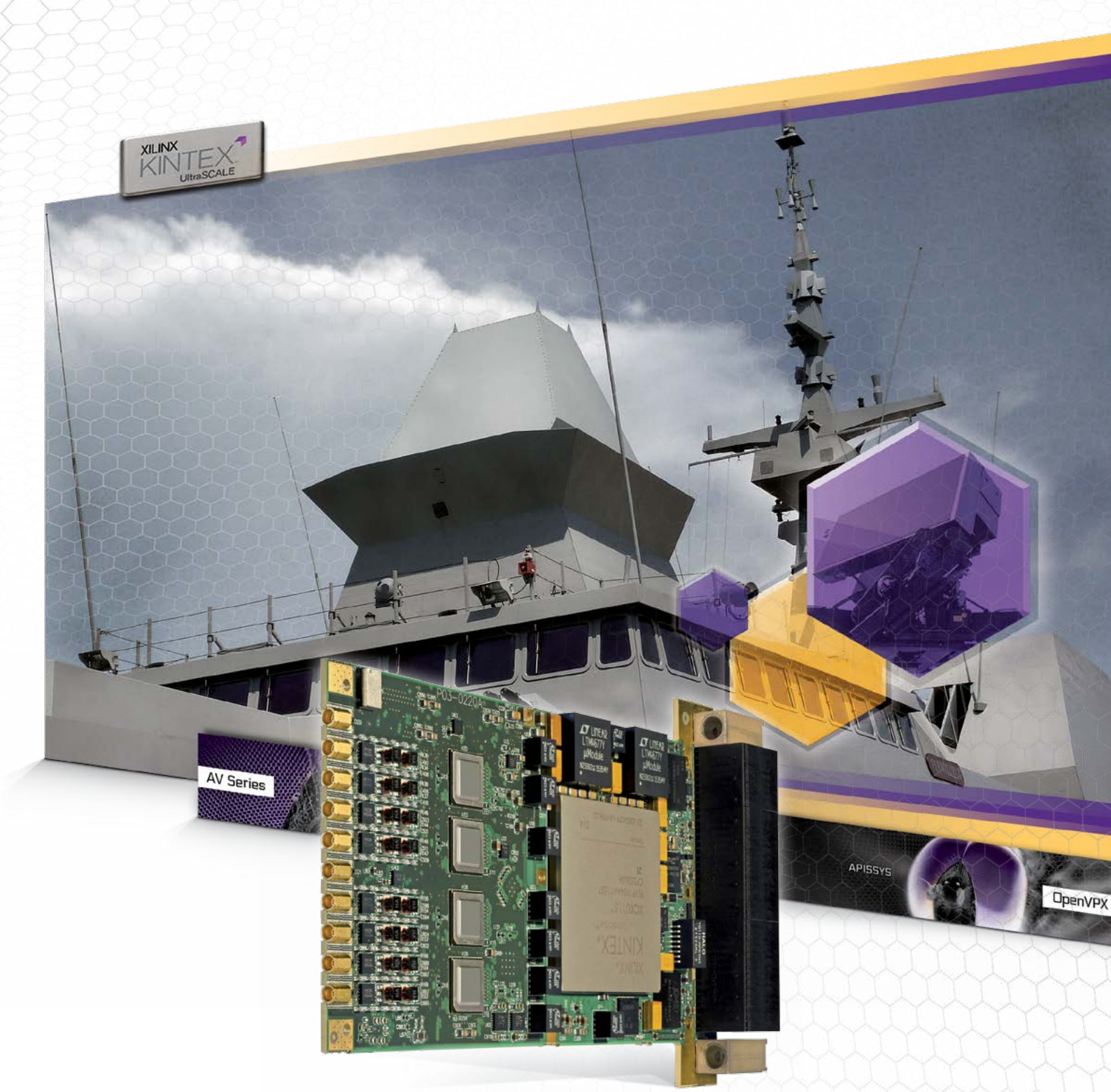


AV 122

Phased-Array Radar Receiver
EW-ESM - MIMO

3U VPX
Kintex UltraScale FPGA
Octal 14 bit 3 Gsps ADC
Conduction or Air-Cooled

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV122

Applications
- Electronic Warfare
- Radar receiver
- Instrumentation
- MIMO

Features
- 8 channels 3 Gsps 14-bit ADC
- Independent Digital Down Converters, decimation factor 2 to 48.
- One Ultra Low jitter clock synthesizers
- External or internal sampling clock
- External and internal sampling clock reference
- User programmable Xilinx® Kintex® Ultrascale™ KU115 FPGA
- 800 MHz 2x 256M64 DDR3 SDRAM
- 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions

Overview
The AV122 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.
The AV122 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.
The AV122 combines eight 14-bit 3 Gsps ADCs with ultra-high processing power delivered by Xilinx® Kintex® Ultrascale™ FPGA, making it ideally suited for fully synchronous multiple channels test and measurement, Electronic Warfare or Ultra-Wideband Radar Receivers applications.
The AV122 features an internal ultra-low jitter reference and one clock synthesizers and can be used with either external clock or external reference for higher flexibility.
The AV122 includes one Xilinx® Kintex® Ultrascale™ KU115 FPGA for an impressive processing capability of more than 7 TMACs (Multiply Accumulate per second), two high speed 256M64 DDR3 SDRAM memory for data processing and two 1 Gb synchronous FLASH memory for multiple firmware storage.
The AV122 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.
The AV122 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

14-bit 3 Gsps Analog-Digital Converters
The AV122 Analog to Digital conversion is performed by four AD9208 dual channel 14-bit 3 Gsps ADCs with independent Digital Down Converters with decimation factor ranging from 2 to 48 in complex mode.
The AV122 provides eight front panel SMPM connectors for analog inputs.
Single ended input signals are AC coupled with an input bandwidth from 1 MHz to more than 9 GHz with 7 dBm input level.
A wideband signal generator is provided for on board, stand-alone calibration

Clock
The AV122 provides one ultra-low jitter clock synthesizers locked on a 100 MHz internal reference.
The AV122 supports a 10 to 800 MHz external reference input either from a front panel SMPM connector or from the VPX P2
Connector. A reference output is available on VPX P2. External clock inputs for the ADCs are supported from either one SMPM connector or VPX P2. External clock from 1.0 GHz to 3.0 GHz are supported (6.0 GHz in divide by 2 mode)
External clock outputs are provided on an SMPM connector and on VPX P2.
Fine phase control is provided on each ADC clock for phase alignment.

Trigger and Synchronization
The AV122 supports a differential pair on VPX P2 connector to be used as trigger or synchronization signal.

FPGA
The AV122 is fitted with a Xilinx® Kintex® Ultrascale™ KU115 user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring sub-system, leaving most of the logic and block RAM and all DSP resources available for customer processing. Dedicated to signal processing, the Xilinx Kintex Ultrascale KU115 FPGA includes 1,451 K logics cells, 2,160 36 Kbit RAM blocs, 6 PCIe interface blocs and 5,520 DSP48 slices for an impressive processing power of more than 7 TMACs.
The FPGA is delivered in -2 speed grade.

Memories
The AV122 includes two 800 MHz 256M64 DDR3 SDRAM memory banks and two 1 Gbit QSPI FLASH used to store multiple FPGA configuration files

VPX interface
The AV122 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV122 also supports 14 TDMS differential pairs plus 8 single ended LVCMOS18 on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.
The AV122 features two low phase noise clock generators able to synthesize clock references for the FPGA GTHs from 60 MHz to 820 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1, 2 and 3, SATA, SRIO and XAUI 10Gbit Ethernet up to 16.375 Gbps.

Microcontroller
The AV122 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.
The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.
The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware
The AV122 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV122 hardware resources.
A base design is provided which demonstrates the use of the AV122 and gives users a starting point for firmware development. The AV122 firmware package is supported on the Xilinx VIVADO® 2017.2 design suite and later.

Software
The AV122 is delivered with software drivers for Windows 7 and Linux.

Ruggedization
The AV122 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4 .

Specifications

Analog Inputs

- Input coupling: AC
  - Input Full power bandwidth: > 9 GHz
  - Full scale : 7 dBm
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion

- Eight channels, Fs ≤ 3 GHz
- Resolution: 14 bit
- Sampling Performances @1 GHz
  - SNR: 59 dBFS
  - SFDR: 70 dBc
  - ENOB: 9.4 bit

Clock

- Internal:
  - One ultra-low jitter clock synthesizers,
  - 1 GHz to 3 GHz low jitter clock
- External Input Clock:
  - Frequency: 1 GHz to 3 GHz (6 GHz in divide by 2)
  - Input level: 10 dBm recommended
  - Connector: SMPM, 50 Ohm and VPX P2
- External reference:
  - frequency: 10 MHz to 800 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

Digital Up and Down Converter

- 2 independent DDC for each ADC:
  - Tuning frequency step: 48-bit NCO
  - DDC with 1/2 to 1/48 decimation ratio with I-Q complex output.

Trigger

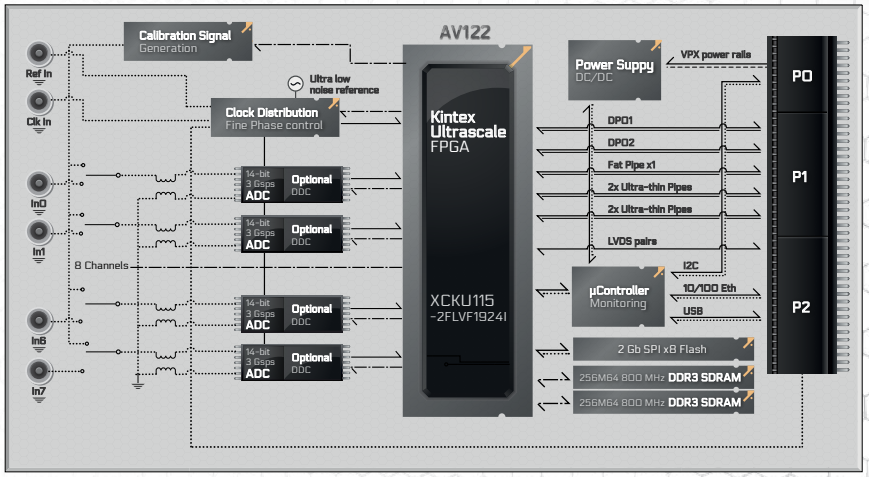
- External: LVDS or LVPECL
  - VPX P2

FPGA

- FPGA: Xilinx Kintex Ultrascale
  - XCKU115-2FLVF1924

Memory

- Two banks 256M64 DDR3 SDRAM, 800 MHz clock
- Two 1 Gbit QSPI FLASH memory



VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 14 TDMS differential pairs
  - 8 single ended LVCMOS18

Software support

- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2017.2 and later

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

Power dissipation (KU 115)

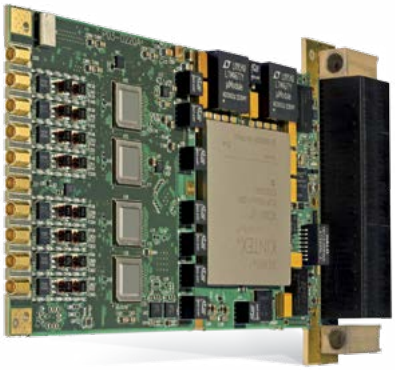
- +12V: 6.7 A max (80W)
- +5V: 9.0 A max (45W)
- +3.3V: 2.1 A max (7W)
- +3.3VAUX: 0.6 A max (2W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ordering information

Part Number		AV122	-	rr	-	a
Ruggedization level	Air Standard	-	-	AS	-	-
	Air Rugged	-	-	AR	-	-
	Conduction Standard	-	-	CS	-	-
	Conduction Rugged	-	-	CR	-	-
Options 1	FPGA Kintex Ultrascale KU115	-	-	-	-	1



Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

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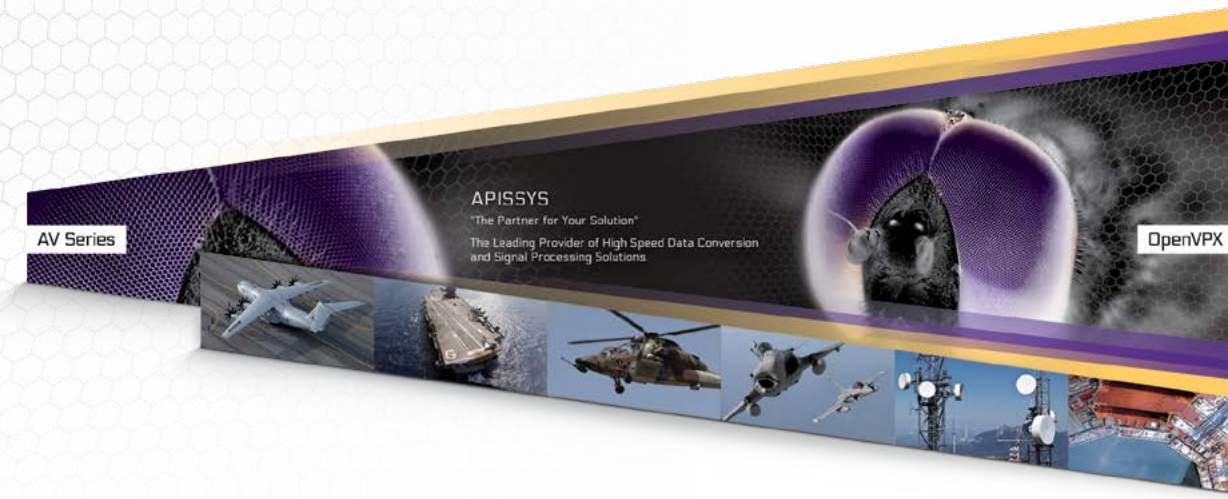
Design By alambiqs.ch - 10.2016



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