XILINX
VIRTEX-7

XILINX
ZYNQ

ARMY WK005

AV Series

APISSYS

OpenVPX

# AV 121

Phased-Array Radar Receiver
EW-ESM

3U VPX
Virtex 7 FPGA
Quad 12 bit 4.0 Gsps ADC
Conduction or Air-Cooled

ApisSys

## Applications

· Phased Array Radar Receiver
· Wideband SAR Radar Receiver
· Electronic Warfare, ESM - RWESM
· Instrumentation
· MIMO

## Features

· 4 channels 4.0 Gsps 12-bit ADC
· 4 independent Digital Down Converters, decimation factor 4 to 32.
· One Ultra Low jitter clock synthesizer
· External or internal clock
· External and internal reference
· External trigger input with TDC
· User programmable Xilinx® Virtex® 7 VX415T or VX690T FPGA
· 667 MHz 256M64 DDR3 SDRAM
· 3U OpenVPX standard compliant
· Air cooled and Conduction cooled rugged versions

## Overview

The AV121 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.

The AV121 is fully compliant with the OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.

The AV121 combines four 12-bit 4.0 Gsps ADCs with ultra-high processing power delivered by Xilinx® Virtex® 7 FPGA, making it ideally suited for fully synchronous multiple channels test and measurement, Electronic Warfare, Ultra Wideband Radar Receivers or MIMO applications.

The AV121 features an internal ultra-low jitter reference and one clock synthesizer and can be used with either external clock or an external reference for higher flexibility.

The AV121 supports an external trigger signal coupled with a 15ps resolution Time to Digital Converter (TDC).

The AV121 includes one Xilinx® Virtex® 7 FPGA VX415T or VX690T for an impressive processing capability of more than 2 TMACs (Multiply Accumulate per second), one high speed 256M64 DDR3 SDRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.

The AV121 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.

The AV121 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

## 12-bit 4.0 Gsps Analog-Digital Converters

The AV121 Analog to Digital conversion is performed by four 12-bit 4.0 Gsps ADCs with independent Digital Down Converters with decimation factor ranging from 4 to 32 in complex mode.

The AV121 provides four front panel SMPM connectors for analog inputs.

Single ended input signals are AC coupled with an input bandwidth from 1 MHz to more than 3.5 GHz with 5 dBm input level.

A wideband signal generator is provided for on board, stand-alone calibration

### Clock

The AV121 provides one ultra-low jitter clock synthesizer locked on a 100 MHz internal reference.

The AV121 supports a 10 to 100 MHz external reference input either from a front panel SMPM connector or from the VPX P2. Connector. A reference output is available on VPX P2. External clock inputs for the ADCs are supported from either one SMPM connector or VPX P2. External clock from 1.0 GHz to 4.0 GHz are supported.

External clock outputs are provided on an SMPM connector and on VPX P2.

Fine phase control is provided on each ADC clock for phase alignment.

### Trigger and Synchronization

The AV121 supports an SMPM connector used as a trigger signal. An embedded Time to Digital Converter with a 15 ps resolution allows for fine synchronization on external events.

## FPGA

The AV121 is fitted with a Xilinx Virtex 7 VX415T or VX690T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring subsystem, leaving most of the logic and block RAM and all DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex 7 VX415T FPGA includes 412,160 logic cells, 880 bloc RAM (36 Kbit each), 2,160 DSP48E1 slices and 2 PCIe interface blocs.

The most powerful version embeds a Xilinx Virtex 7 VX690T which provides 693,120 logic cells, 1,470 bloc RAM and 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACs.

The FPGA is delivered in -2 speed grade.

### Memories

The AV121 includes one 667 MHz 256M64 DDR3 SDRAM memory bank and one 1 Gbit synchronous BPI FLASH used to store multiple FPGA configuration files.

### VPX interface

The AV121 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV121 also supports 24 LVDS differential pairs on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.

The AV121 features two low phase noise clock generators able to synthesize clock references for the FPGA GTXs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 12.5 Gbps.

### Microcontroller

The AV121 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.

The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.

The microcontroller firmware includes all necessary features for board monitoring and supervision.

### Firmware

The AV121 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV121 hardware resources.

A base design is provided which demonstrates the use of the AV121 and gives users a starting point for firmware development. The AV121 firmware package is supported on the Xilinx VIVADO® 2014.4 design suite and later.

### Software

The AV121 is delivered with software drivers for Windows 7 and Linux.

### Ruggedization

The AV121 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions. Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.

# Specifications

## Analog Inputs
- Input coupling: AC
  - Input Full power bandwidth: > 3.5 GHz
  - Full scale : 5 dBm
- Impedance: 50 Ohm
- Connectors: SMPM

## Analog-Digital Conversion
- Quad channels, Fs ≤ 4.0 GHz
- Resolution: 12 bit
- Sampling Performances @1 GHz
  - SNR:     54 dBFS
  - SFDR:   64 dBc
  - ENOB:  8.6 bits

## Clock
- Internal :
  - One ultra low jitter clock synthesizer
  - 1 GHz to 4.0 GHz low jitter clock
- External Input Clocks:
  - Frequency: 1 GHz to 4.0 GHz
  - Input level: 10 dBm recommended
  - Connector: SMPM, 50 Ohm and VPX P2
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

## Digital Up and Down Converter
- Independent DDC on ADC:
  - Tuning frequency step: 32-bit NCO
  - DDC with 1/4 to 1/32 decimation ratio with I-Q complex output.
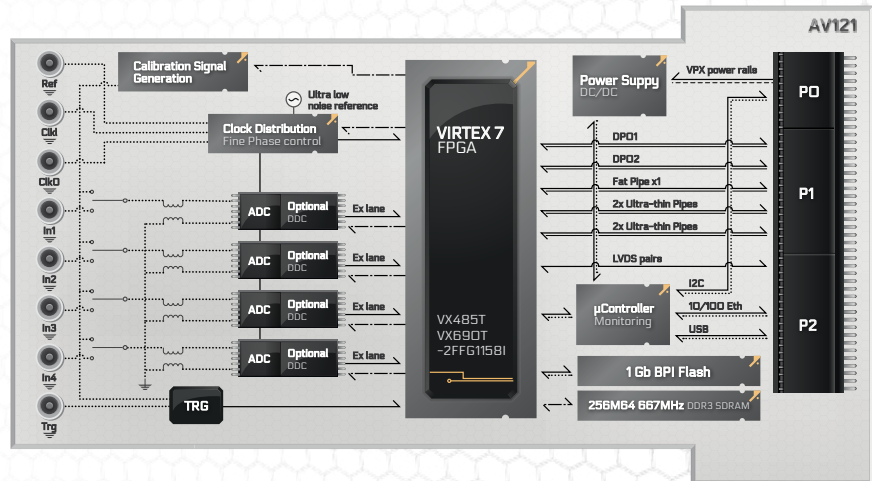
## Trigger
- External: 0 to 2Vp
  - Connector: SMPM, 50 Ohm

## FPGA
- FPGA: Xilinx Virtex 7
  - XC7VX415T-2FFG1158 or
  - XC7VX690T-2FFG1158

## Memory
- 1 bank 256M64 DDR3 SDRAM, 667 MHz clock
- One 1 Gbit NOR FLASH memory

## VPX interface
- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 16 LVDS differential pair

## Software support
- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

## Firmware support
- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2014.4 and later

## Ruggedization
- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

## Power dissipation (690T)
- +12V: 5.8 A max (70W) TBC
- +5V: 9.7 A max (48.40W) TBC
- +3.3V: 0.4 A max (1.3W) TBC
- +3.3VAUX: 0.3 A max (1.1W) TBC

## Weight
- Air cooled : 550g
- Conduction cooled : 650g

# Ordering information

| Part Number | | | AV121 | – | rr | – | a |
|---|---|---|---|---|---|---|---|
| **Ruggedization level** | Air Standard | | – | – | AS | – | – |
| | Air Rugged | | – | – | AR | – | – |
| | Conduction Standard | | – | – | CS | – | – |
| | Conduction Rugged | | – | – | CR | – | – |
| **Options 1** | FPGA Virtex 7 VX415T-2 | | – | – | – | – | 1 |
| | FPGA Virtex 7 VX690T-2 | | – | – | – | – | 2 |

## Ruggedization levels

| | Air flow, Standard<br>AS (VITA 47 EAC4) | Air flow, Rugged<br>AR (VITA 47 EAC6) | Conduction Standard<br>CS (VITA 47 ECC3) | Conduction Rugged<br>CR (VITA47 ECC4) |
|---|---|---|---|---|
| Operating Temperature | 0°C to +55°C<br>(10 CFM airflow sea level) | -40°C to +70°C<br>(20 CFM airflow sea level | -40°C to +70°C<br>(Card Edge) | -40°C to +85°C<br>(Card Edge) |
| Non Operating Temperature | -40°C to +85°C | -50°C to +100°C | -50°C to +100°C | -55°C to +105°C |
| Operating Vibration (Random) | 5Hz - 100Hz +3 dB/octave<br>100Hz-1kHz = 0.04 $g^2$/Hz<br>1kHz - 2kHz -6 dB/octave | 5Hz - 100Hz +3 dB/octave<br>100Hz - 1kHz = 0.04 $g^2$/Hz<br>1kHz - 2kHz -6 dB/octave | 5Hz - 100Hz +3 dB/octave<br>100Hz - 1kHz = 0.1 $g^2$/Hz<br>1kHz - 2kHz -6 dB/octave | 5Hz - 100Hz +3 dB/octave<br>100Hz - 1kHz = 0.1 $g^2$/Hz<br>1kHz - 2kHz -6 dB/octave |
| Operating Shock | 20g, 11 millisecond, half-sine | 20g, 11 millisecond, half-sine | 40g, 11 millisecond, half-sine | 40g, 11 millisecond, half-sine |
| Operating Relative Humidity | 0% to 95%<br>non-condensing | 0% to 95%<br>non-condensing | 0% to 95%<br>non-condensing | 0% to 95%<br>non-condensing |
| Operating Altitude | @ 0 to 10,000 ft<br>with adequate airflow | @ 0 to 30,000 ft<br>with adequate airflow | @ 0 to 30,000 ft | @ 0 to 60,000 ft |
| Conformal Coating | No | Optional (acrylic AVR80) | Yes (default acrylic AVR80) | Yes (default acrylic AVR80) |

# www.apissys.com

Archamps Technopole
60 rue Douglas Engelbart
Bâtiment ABC1 entrée A
F-74160 Archamps, France

Phone: +33 4 50 36 07 58
Fax: +33 4 50 36 05 29