AV 119

Wideband Transceiver with DDC
Radar – MIMO

3U VPX, Virtex 7 FPGA
Dual RF in – dual RF out,
1 GHz instantaneous bandwidth,
4.5 GHz total bandwidth
Conduction or Air-Cooled

ApisSys

Applications

· Wideband Radar transceiver
· Electronic Warfare, COMINT
· Instrumentation
· MIMO

Features

· 2 channels 2.5 Gsps 12-bit ADC
· 2 independent Digital Down Converters, 120 or 140 MHz BW.
· 2 RF out, 16-bit 2.5 Gsps I/Q DAC with Digital Up Converter and RF modulators
· 4 independent Low jitter clock synthesizers and LO
· External and internal reference
· User programmable Xilinx® Virtex® 7 VX415T or VX690T FPGA
· 667 MHz 256M64 DDR3 SDRAM
· 3U OpenVPX standard compliant
· Air cooled and Conduction cooled rugged versions

Overview

The AV119 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.

The AV119 is fully compliant with the OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.

The AV119 combines two 12-bit 2.5 Gsps ADCs plus 2 RF out built on 16-bit 2.5 Gsps I/Q DAC and RF modulators with ultra-high processing power delivered by Xilinx® Virtex® 7 FPGA, making it ideally suited for fully synchronous multiple channels test and measurement, Electronic Warfare, Ultra Wideband Radar Transceivers or MIMO applications.

The AV119 features an internal ultra-low jitter reference and four independent clock synthesizers and can be used with either external clocks or an external reference for higher flexibility.

The AV119 supports an external trigger signal coupled with a 15ps resolution Time to Digital Converter (TDC).

The AV119 includes one Xilinx® Virtex® 7 FPGA VX415T or VX690T for an impressive processing capability of more than 2 TMACs (Multiply Accumulate per second), one high speed 256M64 DDR3 SDRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.

The AV119 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.

The AV119 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

12-bit 2.5 Gsps Analog-Digital Converters

The AV119 Analog to Digital conversion is performed by two 12-bit 2.5 Gsps ADCs with independent 120 or 240 MHz Digital Down Converters.

The AV119 provides two front panel SMPM connectors for analog inputs.

Single ended input signals are AC coupled with an input bandwidth from 1 MHz to more than 5.5 GHz with 9 dBm input level.

16-bit 2.5 Gsps Digital-Analog Converters

The AV119 Digital to Analog conversion is performed by a Quad 16-bit 2.5 Gsps DACs with independent Digital UP Converters.

Two I/Q modulators with more than 1 GHz instantaneous bandwidth allow generation of RF signals from 300 MHz up to 4.5 GHz.

The AV119 provides two front panel SMPM connectors for analog RF outputs.

A loopback mode between RF out and ADC input is provided for on board calibration.

Clock

The AV119 provides four independent ultra-low jitter clock synthesizers locked on a 100 MHz internal reference.

The AV119 provides a front panel SMPM connector for external reference input, 10 to 100 MHz as well as a VPX P2 input. A reference output is available on a front panel SMPM connector and on VPX P2.

Three SMPM connectors support either external clock inputs-outputs for the ADCs and the quad DAC. External clock from 500 MHz to 2.5 GHz are supported.

An SMPM connector supports an external LO for the IQ modulators

Dedicated fine clock phase controls on each synthesizer allow for accurate adjustment of phase delay between all channels.

FPGA

The AV119 is fitted with a Xilinx Virtex 7 VX415T or VX690T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring subsystem, leaving most of the logic and block RAM and all DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex 7 VX415T FPGA includes 412,160 logics cells, 880 bloc RAM (36 Kbit each), 2,160 DSP48E1 slices and 2 PCIe interface blocs.

The most powerful version embeds a Xilinx Virtex 7 VX690T which provides 693,120 logics cells, 1,470 bloc RAM and 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACs.

The FPGA is delivered in -2 speed grade.

Memories

The AV119 includes one 667 MHz 256M64 DDR3 SDRAM memory bank and one 1 Gbit synchronous BPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV119 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV119 also supports 24 LVDS differential pairs on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.

The AV119 features two low phase noise clock generators able to synthesize clock re-ferences for the FPGA GTXs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 12.5 Gbps.

Microcontroller

The AV119 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.

The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.

The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware

The AV119 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV119 hardware resources.

A base design is provided which demonstrates the use of the AV119 and gives users a starting point for firmware development. The AV119 firmware package is supported on the Xilinx VIVADO® 2014.4 design suite and later.

Software

The AV119 is delivered with software drivers for Windows 7 and Linux.

Ruggedization

The AV119 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions. Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.

Specifications

Analog Inputs-Outputs

· Input - Output coupling: AC
  · Input Full power bandwidth: > 5.5 GHz
  · Full scale : 10 dBm
  · Output bandwidth: > 4.5 GHz
· Impedance: 50 Ohm, SMPM

Analog-Digital Conversion

· Two channels, Fs ≤ 2.5 GHz
· Resolution: 12 bit
· Sampling Performances @1 GHz
  · SNR: 58.5 dBFS
  · SFDR: 69 dBc
  · ENOB: 9.3 bits

Digital-Analog Conversion

· Quad 16-bit DAC channels, Fs ≤ 2.5 GHz
· RF IQ modulator instantaneous BW:
  > 1 GHz
  · Noise floor: < -160 dBm/Hz
 · SFDR: 55 dBc on 1 GHz bandwidth

Clock

· Internal :
  · Four independent synthesizers,
  · 1 GHz to 2.5 GHz low jitter clock ADC
    and DAC
  · 400 MHz to 4.1 GHz LO
· External Input/Output Clocks:
  · frequency: 1 GHz to 2.5 GHz for ADC
    and DAC
  · 400 MHz to 4.1 GHz LO input
· External reference:
  · frequency: 10 MHz to 100 MHz
  · Connector: SMPM, 50 Ohm and VPX P2

Digital Up and Down Converter

· Independent DDC on ADC:
  · Tuning frequency step: 10-bit NCO
  · DDC with 1/8 and 1/16 decimation filter.
· Independent DUC on DAC:
  · Tuning frequency step: 48-bit NCO
  · DUC with x1 to x16 interpolation.

Trigger

· External: LVDS or LVPECL
  · VPX P2
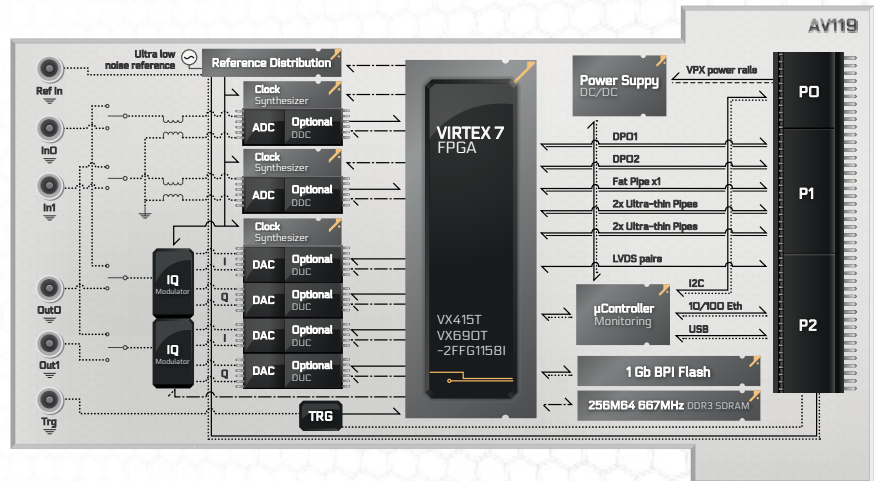
FPGA

· FPGA: Xilinx Virtex 7
  · XC7VX415T-2FFG1158 or
  · XC7VX690T-2FFG1158

Memory

· 1 bank 256M64 DDR3 SDRAM,
  667 MHz clock
· One 1 Gbit NOR FLASH memory

VPX interface

· P1:
  · Data plane: two fat pipes
  · Expansion plane: one fat pipe
  · Control plane: 2 ultra-thin pipes
  · 2 user-defined ultra-thin pipes
· P2:
  · USB2.0 and 10/100 Ethernet
  · 16 LVDS differential pair

Software support

· Software Drivers:
  · Windows 7
  · Linux
· Application example:
  · Windows and Linux

Firmware support

· VHDL cores for all hardware resources
· Base design
· Supported by Xilinx VIVADO 2014.4
  and later

Ruggedization

· As per VITA 47:
  · Air cooled : EAC4 and EAC6
  · Conduction cooled : ECC3 and ECC4

Power dissipation (690T)

· +12V: 6.2 A max (75W) TBC
· +5V: 8.0 A max (40W) TBC
· +3.3V: 0.5 A max (1.6W) TBC
· +3.3VAUX: 0.3 A max (1.1W) TBC

Weight

· Air cooled : 550g
· Conduction cooled : 650g

Ordering information

Part Number		AV119	–	rr	–	a
Ruggedization level	Air Standard	-	-	AS	-	-
	Air Rugged	-	-	AR	-	-
	Conduction Standard	-	-	CS	-	-
	Conduction Rugged	-	-	CR	-	-
Options 1	FPGA Virtex 7 VX415T-2	-	-	-	-	1
	FPGA Virtex 7 VX690T-2	-	-	-	-	2

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (10 CFM airflow sea level)	-40°C to +70°C (20 CFM airflow sea level	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

www.apissys.com

Design By vert-pomme.ch - 01.2015

Archamps Technopole
60 rue Douglas Engelbart
Bâtiment ABC1 entrée A
F-74160 Archamps, France

Phone: +33 4 50 36 07 58
Fax: +33 4 50 36 05 29