AV 113

Phased-Array Radar-Receiver
EW-ESM - MIMO

3U VPX
Virtex 7 FPGA
Octal 14 bit 1.25 Gsps ADC
Conduction or Air-Cooled

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV113

Applications
- Electronic Warfare
- Radar receiver
- LIDAR
- Instrumentation
- MIMO

Features
- 8 channels 1.25 Gsps 14-bit ADC
- 16 independent Digital Down Converters, 1/2 to 1/16 decimation ratio
- 4 independent Low jitter clock synthesizers
- 4 External clock inputs and outputs
- External and internal reference
- External trigger input with TDC
- User programmable Xilinx® Virtex® 7 VX415T or VX690T FPGA
- 667 MHz 256M32 DDR3 SDRAM
- 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions

Overview
The AV113 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.
The AV113 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.
The AV113 combines eight 14-bit 1.25 Gsps ADCs with ultra-high processing power delivered by Xilinx® Virtex® 7 FPGA, making it ideally suited for fully synchronous multiple channels test and measurement, Electronic Warfare, Wideband Radar Receivers or Communication applications.
The AV113 features an internal ultra-low jitter reference and four independent clock synthesizers and can be used with either external clocks or external reference for higher flexibility.
The AV113 supports an external trigger signal coupled with a 15ps resolution Time to Digital Converter (TDC).
The AV113 includes one Xilinx® Virtex® 7 FPGA VX415T or VX690T for an impressive processing capability of more than 2 TMACs (Multiply Accumulate per second), one high speed 256M32 DDR3 SDRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.
The AV113 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.
The AV113 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

14-bit 1.25 Gsps Analog-Digital Converters
The AV113 Analog to Digital conversion is performed by eight 14-bit 1.25 Gsps ADCs with independent Digital Down Converters.
The AV113 provides eight front panel SMPM connectors for analog inputs.
Single ended input signals are AC coupled with an input bandwidth from 1 MHz to more than 2.3 GHz with 10 dBm input level.
A wideband signal generator is provided for on board, stand-alone calibration.

Clock
The AV113 provides four independent ultra-low jitter clock synthesizers locked on a 100 MHz internal reference.
The AV113 provides a front panel SMPM connector for external reference, 10 to 100 MHz as well as a VPX P2 reference input.
The VPX P2 connector also supports either external clock inputs for the ADCs or clock outputs when the internal clock synthesizers are used. External clock from 500 MHz to 1.25 GHz are supported.
Dedicated fine clock phase controls on each pair of channels allow for accurate adjustment of phase delay between all channels.

Trigger and Synchronization
The AV113 support a differential pair on VPX P2 connector used a trigger signal. An embedded Time do Digital Converter with a 15 ps resolution allow for fine synchronisation on external event.

FPGA
The AV113 is fitted with a Xilinx Virtex 7 VX415T or VX690T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring subsystem, leaving most of the logic and block RAM and all DSP resources available for customer processing.
Dedicated to signal processing, the Xilinx Virtex 7 VX415T FPGA includes 412,160 logics cells, 880 bloc RAM (36 Kbit each), 2,160 DSP48E1 slices and 2 PCIe interface blocs.
The most powerful version embeds a Xilinx Virtex 7 VX690T which provides 693,120 logics cells, 1,470 bloc RAM and 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACs.
The FPGA is delivered in -2 speed grade.

Memories
The AV113 includes one 667 MHz 256M32 DDR3 SDRAM memory banks and one 1 Gbit synchronous BPI FLASH used to store multiple FPGA configuration files.

VPX interface
The AV113 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV113 also supports 16 LVDS differential pairs on P2 plus USB2.0 and 10/100 Ethernet for supervision and monitoring.
The AV113 features two low phase noise clock generators able to synthesize clock references for the FPGA GTXs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 12.5 Gbps.

Microcontroller
The AV113 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.
The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.
The microcontroller firmware includes all necessary features for board monitoring and supervision.

Firmware
The AV113 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV113 hardware resources.
A base design is provided which demonstrates the use of the AV113 and gives users a starting point for firmware development. The AV113 firmware package is supported on the Xilinx VIVADO® 2013.4 design suite and later.

Software
The AV113 is delivered with software drivers for Windows 7 and Linux.

Ruggedization
The AV113 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.

Specifications

Analog Input

- Input coupling: AC
  - Full power bandwidth: > 2.3 GHz
  - Full scale: 10 dBm
- Impedance: 50 Ohm
- Connectors: SMPM

Analog-Digital Conversion

- Eight channels
  - Fs ≤ 1.25 GHz, -AS version
  - FS ≤ 1.1 GHz, -AR, -CS and -CR versions
- Resolution: 14 bit
- Sampling Performances @1 GHz
  - SNR: 65 dBFS
  - SFDR: 76 dBc
  - ENOB: 10.1 bit

Clock

- Internal:
  - Four independent synthesizers,
  - 500 MHz to 1.25 GHz low jitter clock
- External Input/Output Clocks:
  - frequency: 500 MHz to 1.25 GHz
  - LVDS or LVPECL differential pairs on VPX P2
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: SMPM, 50 Ohm and VPX P2

Digital Down Converter

- 16 independent DDC:
  - Tuning frequency step: 12-bit NCO
  - DDC with 1/2 to 1/16 decimation

Trigger

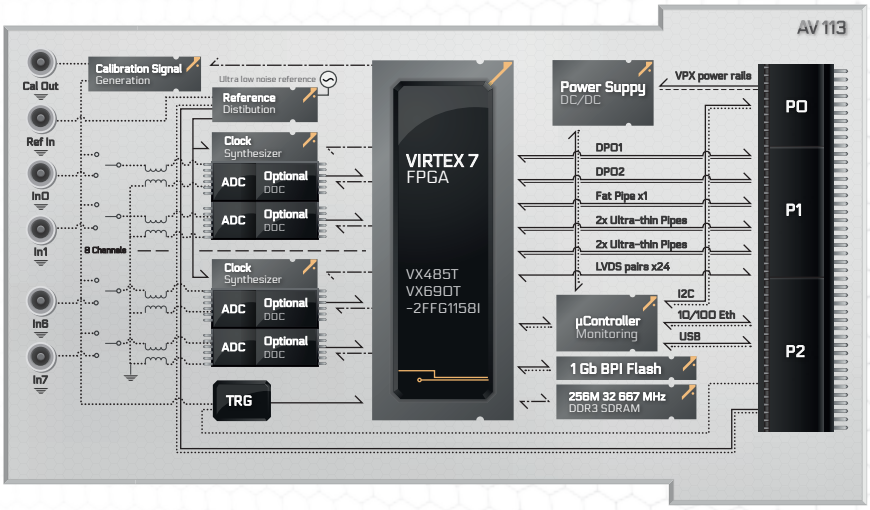
- External: LVDS or LVPECL
  - VPX P2

FPGA

- FPGA: Xilinx Virtex 7
  - XC7VX415T-2FFG1158 or
  - XC7VX690T-2FFG1158

Memory

- 1 bank 256M32 DDR3 SDRAM, 667 MHz clock
- One 1 Gbit NOR FLASH memory



VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 16 LVDS differential pair
  - ADCs input and output sampling clocks

Software support

- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2013.4 and later

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

Power dissipation (690T)

- +12V: 6.2 A max (75W)
- +5V: 8.0 A max (40W)
- +3.3V: 0.5 A max (1.6W)
- +3.3VAUX: 0.3 A max (1.1W)

Weight

- Air cooled : 550g
- Conduction cooled : 650g

Ordering information

Part Number		A	V	113	-	rr	-	a
Ruggedization level	Air Standard	-	-	-	-	AS	-	-
	Air Rugged	-	-	-	-	AR	-	-
	Conduction Standard	-	-	-	-	CS	-	-
	Conduction Rugged	-	-	-	-	CR	-	-
Options 1	FPGA Virtex 7 VX415T-2	-	-	-	-	-	-	1
	FPGA Virtex 7 VX690T-2	-	-	-	-	-	-	2

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (1) (10 CFM airflow at sea level)	-40 to +70°C (1) (20 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

www.apissys.com

Design By vert-pomme.ch - 09.2013

ApisSys
Archamps Technopole
60 rue Douglas Engelbart
Bâtiment ABC1 entrée A
F-74160 Archamps, France
Phone: +33 4 50 36 07 58
Fax: +33 4 50 36 05 29