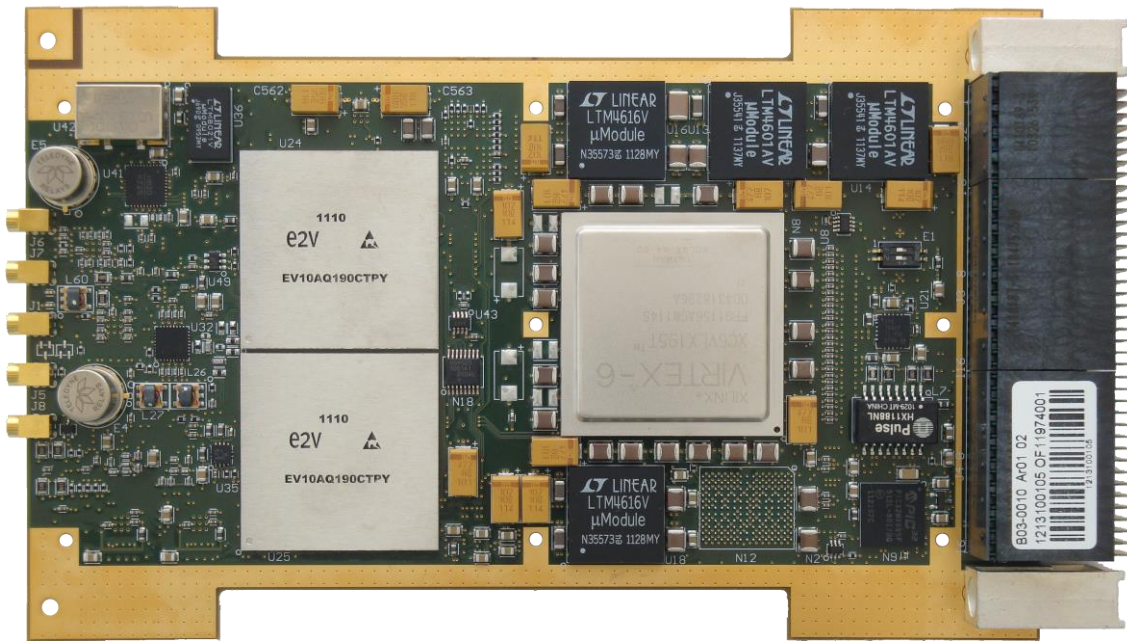# AV101

10-bit 10 GSPS ADC and Signal processing 3U VPX Board

Applications

- Real time processing
- Electronic Warfare
- Radar receiver
- LIDAR
- Instrumentation

Features

- 1 channel 10-bit, 10 Gsps ADC
- External clock and reference input
- Low jitter internal clock generation
- External trigger input with 20ps TDC
- User programmable Xilinx® Virtex® 6 LX195T/SX475T FPGA
- 350 MHz 2M x 36 QDRII+ SRAM
- USB 2.0 and 10/100 Ethernet for stand alone applications
- 3U VPX form factor
- Air cooled and Conduction cooled rugged versions
- FPGA firmware cores
- Windows® and Linux® drivers

Overview

The AV101 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.

The AV101 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAUI 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.

The AV101 combines the highest performances 10-bit 10 Gsps ADC with ultra high processing power delivered by Xilinx® Virtex® 6 FPGA, making it ideally suited for test and measurement, Electronic Warfare, Ultra Wideband Radar Receivers or LIDAR applications.

The AV101 features an internal ultra low jitter reference and clock generation and can be used with either external clock or external reference for higher flexibility.

The AV101 supports an external trigger signal used to synchronize processing with external events.

The AV101 includes one Xilinx® Virtex® 6 FPGA LX195T/LX240T/SX315T or SX475T for an impressive processing capability of up to 1 TMACs (Multiply Accumulate per second), one high speed 2M36 QDRII+ SRAM memory for data processing and one FLASH memory for multiple firmware storage.

The AV101 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and in stand alone mode.

The AV101 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.
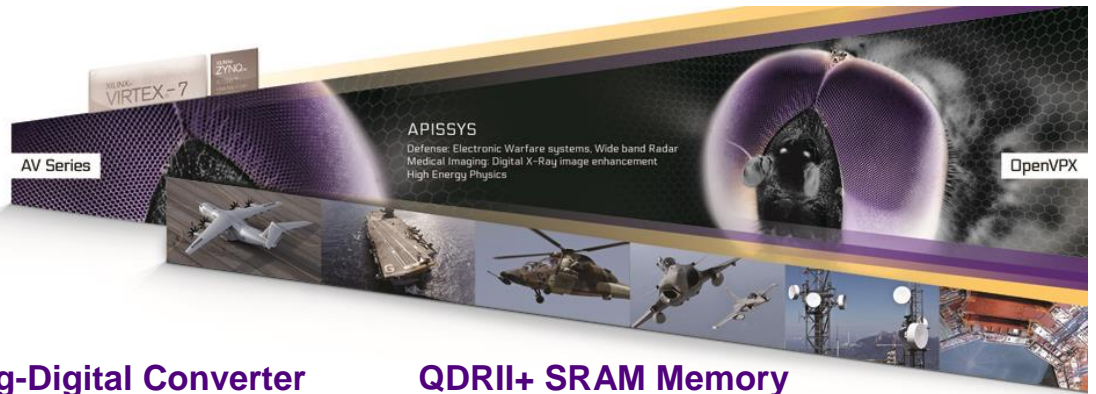
10-bit 10 Gsps Analog-Digital Converter

The AV101 Analog to Digital conversion is performed by a 10-bit 10 Gsps ADC using multiple ADCs interleaving technologies.

The AV101 provides one front panel MMCX connector for analog input.

Single ended input signal is AC or DC coupled (assembly option) with an input bandwidth from DC to more than 3 GHz with 2 dBm input level.

A wideband signal generator is provided for on board, stand-alone calibration.

Clock

The AV101 provides an internal ultra low jitter clock generator locked on a 100 MHz internal reference.

The AV101 provides a front panel MMCX connector for external reference, 10 to 100 MHz, a front panel MMCX connector for an external clock input, from 1.8 GHz to 2.5 GHz (1/4 of sampling rate) and a front panel MMCX for an external clock output.

A dedicated fine clock phase control allows for accurate adjustment of phase delay between interleaved ADCs.

Trigger and Synchronization

The AV101 provides a front panel MMCX connector for external trigger input coupled with a 15 ps resolution TDC.

FPGA

The AV101 is fitted with a Xilinx Virtex 6 LX195T/LX240T/SX315T or SX475T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as QDRII+ SRAM and monitoring sub-system, leaving most of the logic, block RAM and DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex 6 LX195T FPGA includes 199,680 logics cells, 344 bloc RAM (36 Kbit each), 640 DSP48E1 slices, 2 PCIe interface blocs and 4 10/100/1000 Ethernet MAC blocs. The most powerful version embeds a Xilinx Virtex 6 SX475T which provides 476,160 logics cells, 1,064 bloc RAM and 2,016 DSP48E1 slices for an impressive processing power of up to 1 TMACs.

The FPGA is delivered in -2 speed grade.

QDRII+ SRAM Memory

The AV101 includes one 2M36 QDRII+ SRAM memory clocked at 350 MHz for a peak data rate of 6.3 GB par second.

FLASH Memory

The AV101 includes one 1 Gbit BPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV101 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1.

The AV101 also supports a USB2.0, a 10/100 Ethernet and 28 LVDS differential pairs on P2.

Firmware

The AV101 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV101 hardware resources.

A base design is provided which demonstrates the use of the AV101 and gives users a starting point for firmware development.

The AV101 firmware package is supported on the Xilinx ISE[®] 13 design suite and later versions.
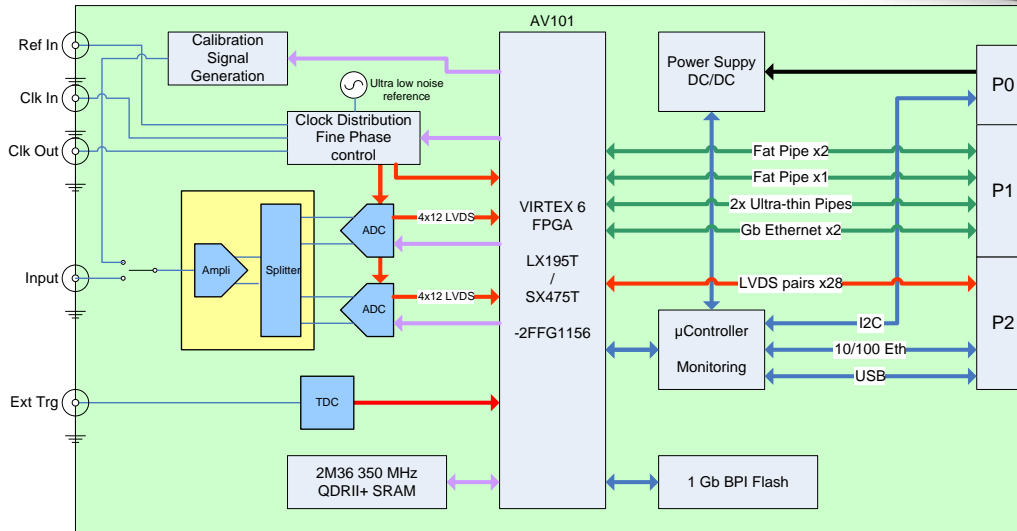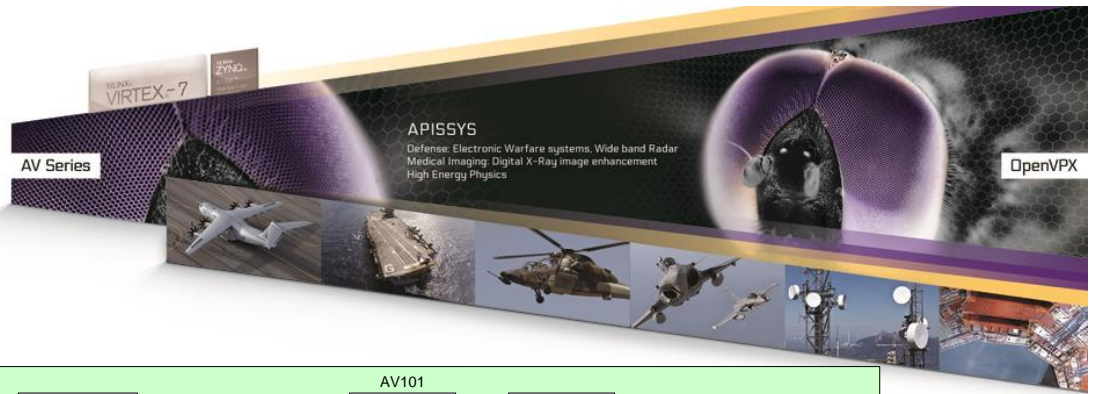
Software

The AV101 is delivered with software drivers for Windows 7 and Linux.

An application example is provided.

Ruggedization

The AV101 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6 and ECC3.

Specifications

Analog Input

- Input coupling: AC or DC
  - Full power bandwidth: > 3 GHz
  - Full scale : 2 dBm
- Impedance: 50 Ohm
- Connector: MMCX

Analog-Digital Conversion

- Single channel
- Resolution: 10 bit
- Sampling Frequency: ≤ 10 GHz
- Sampling Performances @1 GHz
  - SNR: 48 dBFS
  - SFDR: 45 dBc
  - ENOB: 7.2 bits

Clock

- Internal: 2.2 to 2.5 GHz low jitter clock (1/4 sampling clock)
- External Input Clock:
  - frequency: 1.8 GHz to 2.5 GHz
  - Connector: MMCX, 50 Ohm
- External Output Clock:
  - frequency: max 2.5 GHz
  - Connector: MMCX, 50 Ohm
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: MMCX, 50 Ohm

Trigger

- External: 0 to 2Vp
  - Connector: MMCX
  - TDC resolution: ≈ 15ps
  - TDC standard deviation: ≈ 15ps

FPGA

- FPGA: Xilinx Virtex 6
  - XC6VLX195T-2FFG1156 or
  - XC6VLX240T-2FFG1156 or
  - XC6VSX315T-2FFG1156 or
  - XC6VSX475T-2FFG1156

Memory

- 1 bank 2M x 36-bit QDRII+ SRAM, 350 MHz clock
- One 1 Gbit NOR FLASH memory used in 8-bit BPI mode

VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 28 LVDS differential pairs

Software support

- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx ISE 13 and later
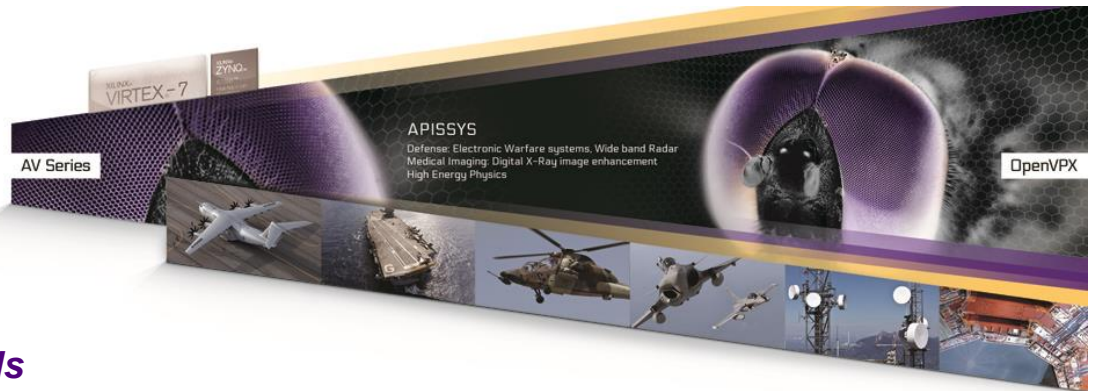
Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3

Power dissipation

- +12V: 2.9 A max (35.4W)
- +5V: 6.3 A max (31.7W)
- +3.3V: 0.7 A max (2.3W)
- +3.3VAUX: 0.2 A max (0.7W)

Weight

- Air cooled : 500g
- Conduction cooled : 500g

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (1) (8 CFM airflow at sea level)	-40 to +70ºC (1) (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic 1B31)	Yes (default acrylic 1B31)	Yes (default acrylic 1B31)

Ordering information

Part Number		A V 101 -	rr	-	a	b
Ruggedization level	Air Standard		AS			
	Air Rugged		AR			
	Conduction Standard		CS			
	Conduction Rugged		CR			
Options 1	FPGA Virtex 6 LX195T-2				1	
	FPGA Virtex 6 LX240T-2				2	
	FPGA Virtex 6 SX315T-2				3	
	FPGA Virtex 6 SX475T-2				4	
Options 2	AC coupled					1
	DC coupled					2

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