New!

Model 5950

8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX

QUARTZ

NAVIGATOR Design Suite

Features

- Supports Xilinx Zynq UltraScale+ RFSoC FPGAs
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- LVDS connections to the Zynq UltraScale+ FPGA for custom I/O
- Optional VITA-66.4 optical interface for backplane gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4, VITA-57.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available
- Unique QuartzXM eXpress Module enables migration to other form factors

General Information

The Quartz Model 5950 is a high-performance 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoC FPGA. The RFSoC integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The Model 5950 brings RFSoC performance to 3U VPX with a complete system on a board.

Complementing the RFSoC's on-chip resources are the 5950's sophisticated clocking section for single board and multi-board synchronization, a low-noise front end for RF input and output, up to 16 GBytes of DDR4, a PCIe interface, a gigabit serial optical interface capable of supporting dual 100 GigE connections and general purpose serial and parallel signal paths to the FPGA.

Board Architecture

The 5950 board design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Pentek developed IP and software functions utilize this architecture to provide data capture, timing, and interface solutions for many of the most common application requirements.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits (FDK) include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5950's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 5950 either from applications running locally on the ARMs, or using the Navigator API, control and command from remote system computers.

A/D Converter Stage

The front end accepts analog IF or RF inputs on eight front panel MMCX connectors with transformer-coupling into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A Converter Stage

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x , 4x and 8x. Each D/A output is transformer coupled to a front panel MMCX connector.

Clocking and Synchronization

The 5950 front panel includes inputs for sample clock, reference clock, reference sync and gate/trigger. In addition to the front panel, these same signals are also available on the VPX P2 connector for distribution through the backplane.

The on-board timing bus generator uses these signals, in addition to a frequency synthesizer, to create the required A/D and D/A clocks and a SysRef for operation of the data converters. The timing bus generator supports an internal clock mode where the sample clock is driven by the programmable frequency synthesizer and no additional clock needs to be provided. In an alternate mode, the on-board sample clock can be synchronized to a 10 MHz reference clock received either through a front panel connector or the VPX P2 connector. The Model 5950 can also accept an external sample clock through a front panel connector or through the VPX P2 connector. This mode bypasses the on-board sample clock.

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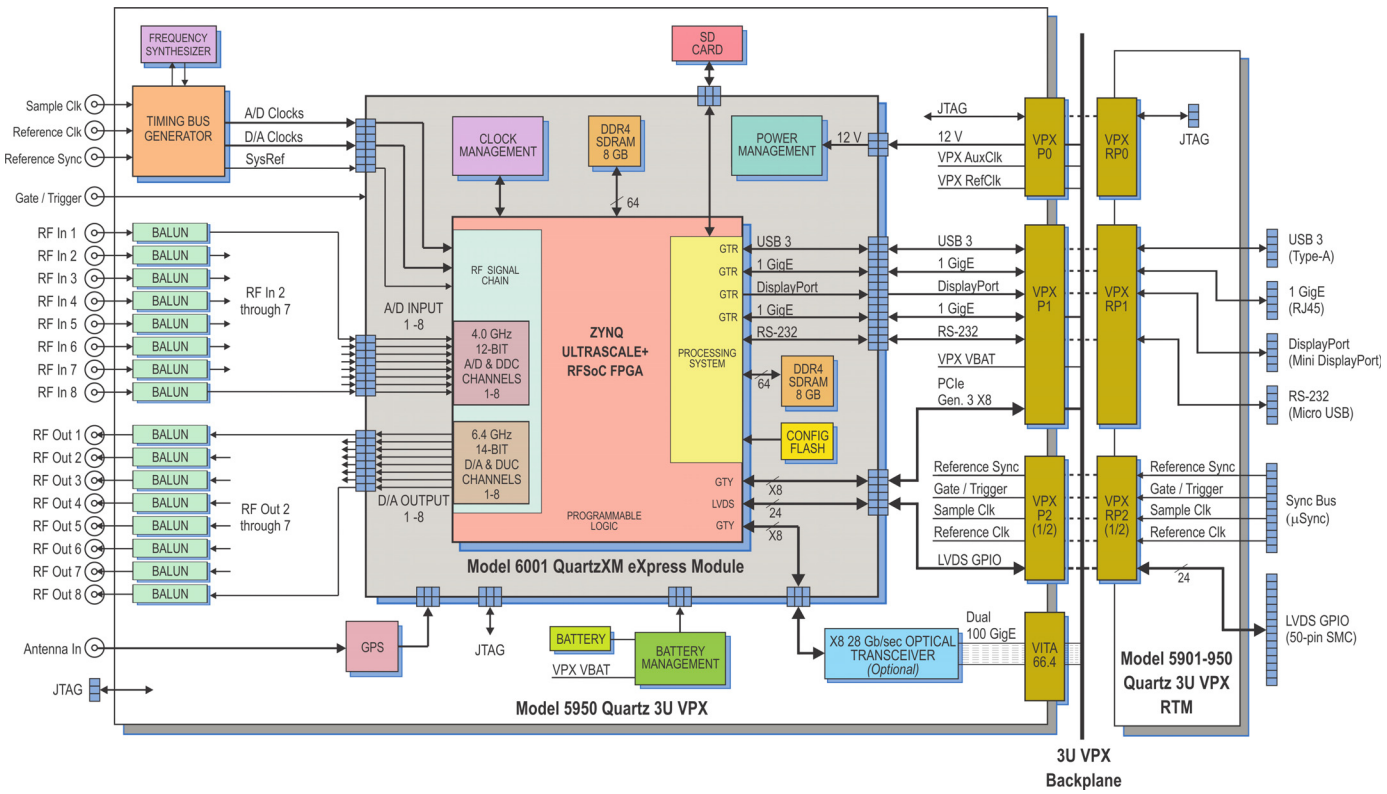
Model 5950

8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX



A multi-function gate/trigger input is available on the front panel as well as the VPX P2 connector for external control of data acquisition and playback.

Expandable I/O

The Model 5950 supports the VITA-66.4 standard providing up to eight 28 Gb/sec full duplex optical lanes to the backplane. With the built-in 100 GigE UDP interface or installation of user provided serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

12 pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O.

Memory Resources

The 5950 architecture supports up 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which, along with the Pentek supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

An 8 GByte bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

PCI Express Interface

The Model 5950 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

GPS

An optional GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and 10 MHz reference clock to the FPGA.

Rear Transition Module

The Model 5901 RTM compliments the 5950 by providing rear backplane access to standard interfaces including: JTAG, USB 3, 1 GigE, DisplayPort and RS-232. The RTM also includes Pentek's µSync connector for synchronizing multiple boards, and a general purpose FPGA I/O connector that provides access to 12 LVDS pairs from the FPGA.

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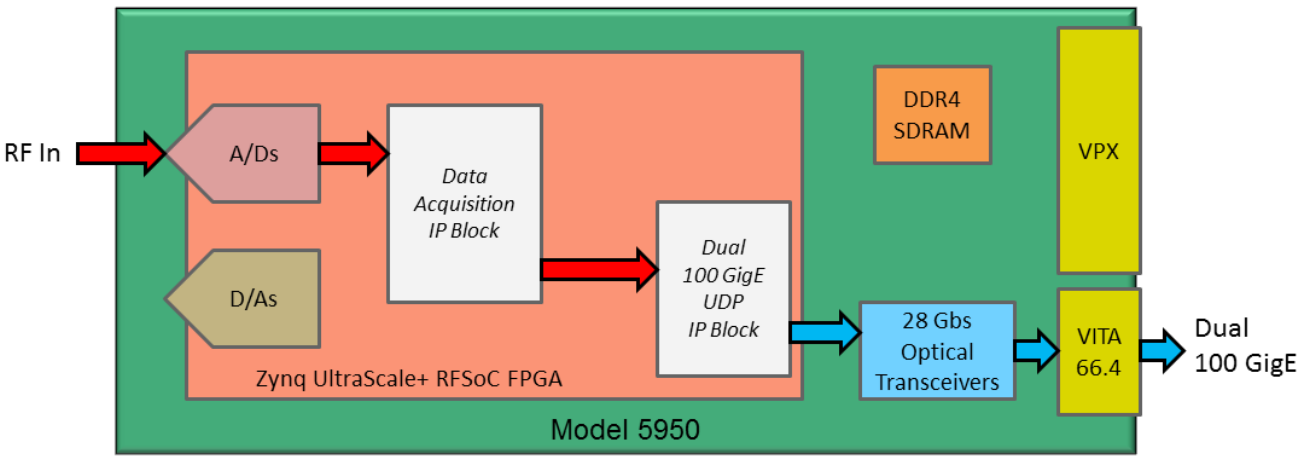
Optimized IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Pentek helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications. For each example that follows the board's included IP is all that is needed to demonstrate the application and may satisfy the full set of requirements for any particular application. These applications can also be the starting point for adding additional IP from the Pentek Navigator IP library or for adding custom IP.

Example Application 1 - High Bandwidth Data Streaming

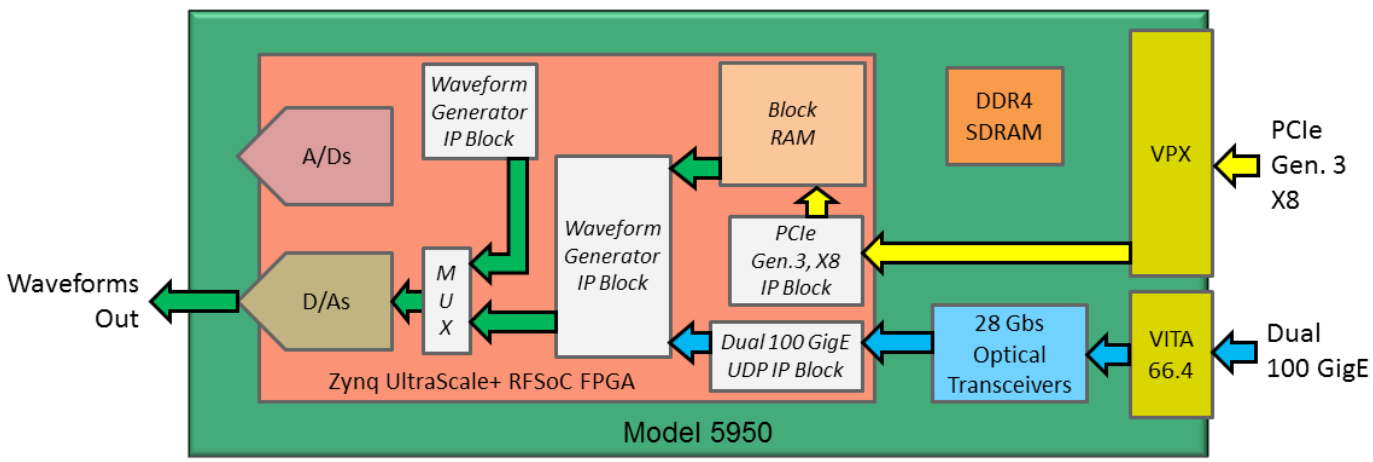
The RFSoC's eight 4 GSPS A/Ds are capable of producing an aggregate data rate of 64 GBytes/sec when all channels are enabled. While capturing this much raw data is not feasible, the A/Ds built-in digital down converters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage components downstream in the system.

In some applications capturing the raw, full bandwidth data is crucial. The 5950's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board. Along with the built-in data acquisition IP, the 5950 can stream two full bandwidth A/D data streams over optical cable to a downstream storage or processing subsystem.



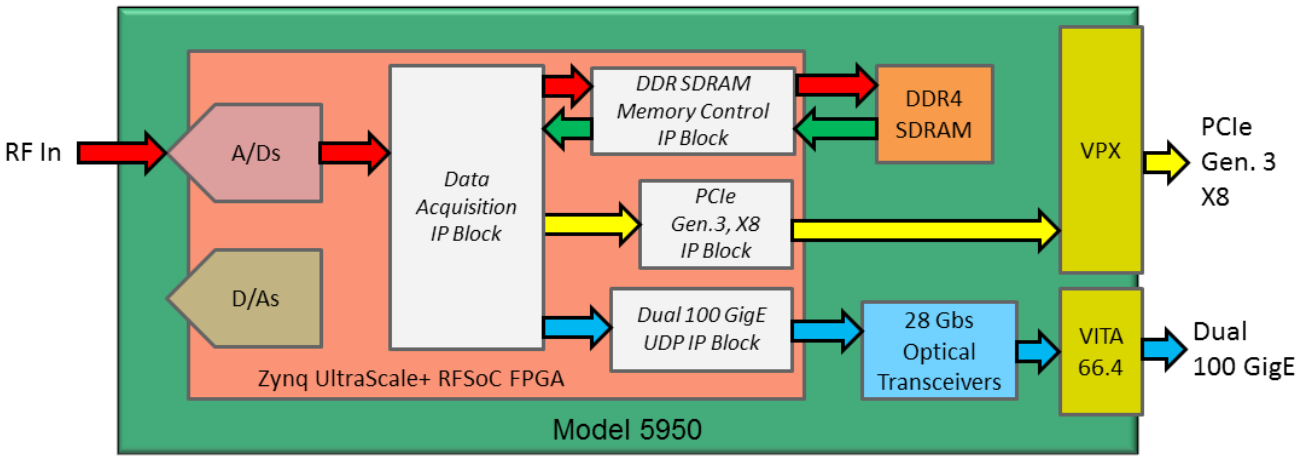
Example Application 2 - Waveform Generator

The 5950's IP includes a flexible waveform generator engine. Multiple waveforms can be loaded into the 5950's RFSoC's Block RAM through the PCIe interface. These waveforms can then be output through the D/As based on user programmed sequences and triggers. In an alternate mode, waveforms can be streamed directly to the D/As via the 100 GigE interface.



Example Application 3 - Multi-mode Data Acquisition System

In some applications multiple data acquisition modes may need to be operated at the same time. A required dataflow could be full bandwidth streaming of a single A/D channel over 100 GigE to a data recorder while another channel of A/D data is stored as snapshots in the boards DDR4 SDRAM and read by the ARM processor while yet other A/D channels are down converted using the A/Ds' built-in DDCs and streamed over PCIe. The 5950 provides these modes with built-in IP supporting complex data streaming scenarios without the need for creating custom IP.

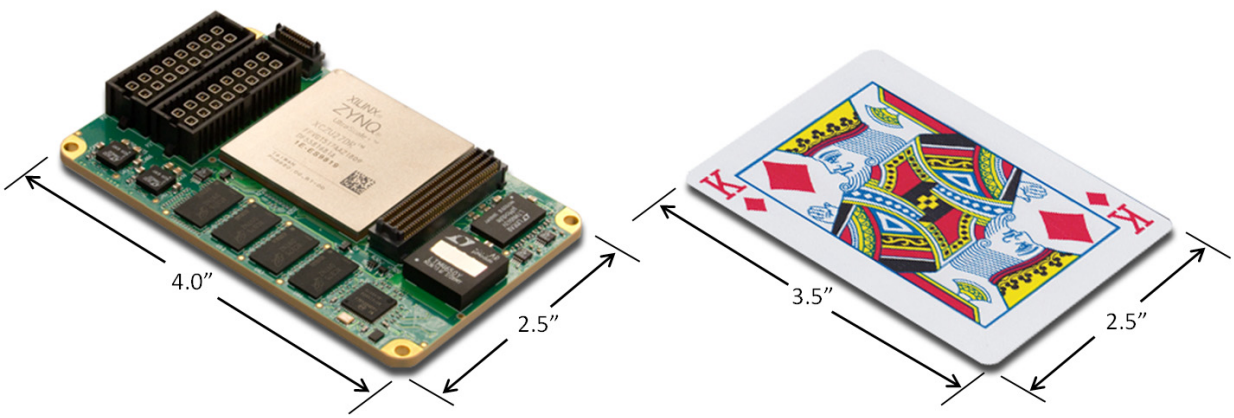


Flexible Modular Design

While the Model 5950 follows the form factor of a standard 3U OpenVPX board, the unique modular design of Pentek's Model 6001 QuartzXM eXpress Module provides the flexibility to deploy this solution in many different situations. The heart of the QuartzXM is a system on module containing all of the key components including the RFSoC FPGA, DDR4 SDRAM, and power and clock management.

In the case of the 5950 the QuartzXM is mounted on a 3U OpenVPX carrier which complements the design with a timing bus generator, analog signal conditioning, a GPS receiver and an 8x 28 Gbps optical transceiver. As a module and carrier board set, the 5950 becomes a complete, ready to deploy 3U OpenVPX solution available for a range of operating environments from commercial to rugged and conduction cooled.

The Model 6001 QuartzXM can also be mounted on other carriers available from Pentek to support standard form factors, or for applications that require a non-standard footprint, Pentek supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best in class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application specific carrier design.



Model 6001 QuartzXM eXpress Module

8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX

Specifications - Model 5950

Field Programmable Gate Array
- **Type: (standard)** Xilinx Zynq UltraScale+ RFSoC XCZU27DR
  Option 028: Xilinx Zynq UltraScale+ RFSoC XCZU28DR
- **Speed: (standard)** -1 speed grade
  Option 002: -2 speed grade

RFSoC RF Signal Chain
- **Front Panel Analog Inputs:**
  - **Quantity:** 8
  - **Connectors:** MMCX
  - **Input Type:** Transformer-coupled
  - **Transformer Type:** Mini-Circuits TCM1-83X+
  - **Full Scale Input:** +4 dBm into 50 ohms (includes matching network)
  - **3 dB Passband:** 10 MHz to 4000 MHz
- **A/D Converters:**
  - **Quantity:** 8
  - **Sampling Rate:** 4.0 GHz
  - **Resolution:** 12 bits
- **Digital Downconverters:**
  - **Quantity:** 1 per A/D
  - **Decimation Range:** 1x, 2x, 4x and 8x
  - **LO Tuning Freq. Resolution:** 48 bits, 0 to f_s
  - **Filter:** 80% pass band, 89 dB stop-band attenuation
- **Front Panel Analog Outputs:**
  - **Quantity:** 8
  - **Connectors:** MMCX
  - **Input Type:** Transformer-coupled
  - **Transformer Type:** Mini-Circuits TCM1-83X+
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 10 MHz to 4000 MHz
- **D/A Converters:**
  - **Quantity:** 8
  - **Sampling Rate:** 6.4 GHz
  - **Resolution:** 14 bits
- **Digital Upconverters:**
  - **Quantity:** 1 per D/A
  - **Interpolation Range:** 1x, 2x, 4x and 8x
  - **LO Tuning Freq. Resolution:** 48 bits
  - **Filter:** 80% pass band, 89 dB stop-band attenuation
- **Sample Clock Source:** On-board programmable clock source or extrenal clock source received on front panel MMCX connector or on VPX-P2
- **Reference Clock, Reference Sync and Gate/Trigger:** Received on front panel MMCX connectors or on VPX-P2

RFSoC RF Processing System
- **ARM Cortex-A53:**
  - **Quantity:** 4
  - **Speed:** 1.5 GHz
- **ARM Cortex-R5:**
  - **Quantity:** 2
  - **Speed:** 600 MHz

Custom FPGA I/O
- **Parallel:** 12 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Optical (Option 110):** VITA-66.4, 8X full duplex lanes @ 28 Gb/sec

Memory
- **Processing System:**
  - **Type:** DDR4 SDRAM
  - **Size: (standard)** 4 GBytes;
    Option 150: 8 GBytes
  - **Speed:** 1200 MHz (2400 MHz DDR)
- **Programmable Logic:**
  - **Type:** DDR4 SDRAM
  - **Size: (standard)** 4 GBytes;
    Option 150: 8 GBytes
  - **Speed:** 1200 MHz (2400 MHz DDR)
  - **FPGA Configuration FLASH:** 2x 1 Gbit QSPI

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option 702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option 763: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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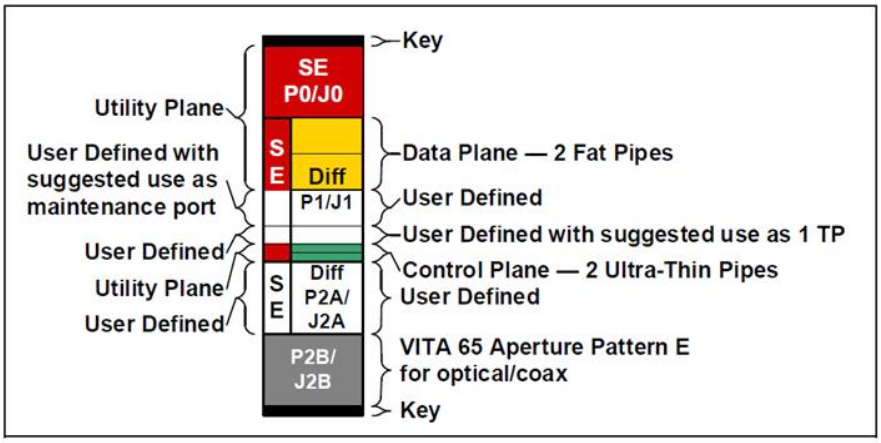
OpenVPX Compatibility: The Model 5950 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F2U1E-14.6.10-n

Model 8257

The Model 8257 is a 1-Slot 3U VPX chassis. Offered as a convenient, low cost solution for hosting the 5950, it includes power and cooling to match the 5950's requirements in a portable desk top package.



Ordering Information

Model	Description
5950	8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX
Options:	
-002	-2 FPGA speed grade, -1 standard
-011	Multi-board synchronization support
-028	XCZU28DR FPGA, XCZU27DR standard
-110	VITA-66.4 8X optical interface
-150	8 GBytes processor system memory, 8 GBytes programmable logic memory
-180	GPS support
-702	Air cooled, Level L2
-763	Conduction cooled, Level L3

Model	Description
5901	Rear Transition Module - 3U VPX
Option:	
-950	Support for Model 5950

Model	Description
8257	1-Slot 3U VPX Development Chassis

Specifications - Model 5901 RTM

Rear Panel Connections:

USB 3:
Connector Type: Type-A
Quantity: 1

1 GigE:
Connector Type: RJ45
Quantity: 1

DisplayPort:
Connector Type: Mini DisplayPort
Quantity: 1

RS-232:
Connector Type: Micro USB
Quantity: 1

Sync Bus:
Connector Type: µSync
Quantity: 1
Signals: Sample Clock, Reference Clock, Reference Sync, Gate/Trigger

FPGA GPIO:
Connector Type: 50-pin SMC
Quantity: 1
Signals: 12 LVDS pairs

Additional Connections:

JTAG:
Connector Type: 2x7 pin, 2mm pitch header, Xilinx JTAG standard pin-out
Quantity: 1

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